

MODEL NAME : *ANREDB4100*  
PCB NO : *LA-G441P*  
BOM P/N : *431ACQ31L\**

# Dell/Compal Confidential

## Schematic Document

### (Spyglass Whiskey Lake U)

**BOM Structure**

- 128M@ : 128M SPI ROM
- 256M@ : 256M SPI ROM
- @ : Nopop Component
- RF@ : RF Component
- @RF@ : RF Nopop Component
- EMC@ : EMI Component
- @EMC@ : EMI Nopop Component
- 5105@ : Option for MEC5105
- 5106@ : Option for MEC5106
- ST@ : ST TPM
- 750@ : Nuvoton TPM
- NRTD3@ : non RTD3 support
- RTD3@ : RTD3 support
- NDS3@ : non Deep sleep support
- DS3@ : Deep sleep support
- XDP@ : XDP Component
- DB@ : Debug Component
- BreakDown@ : Breakdown Component

2018-09-28

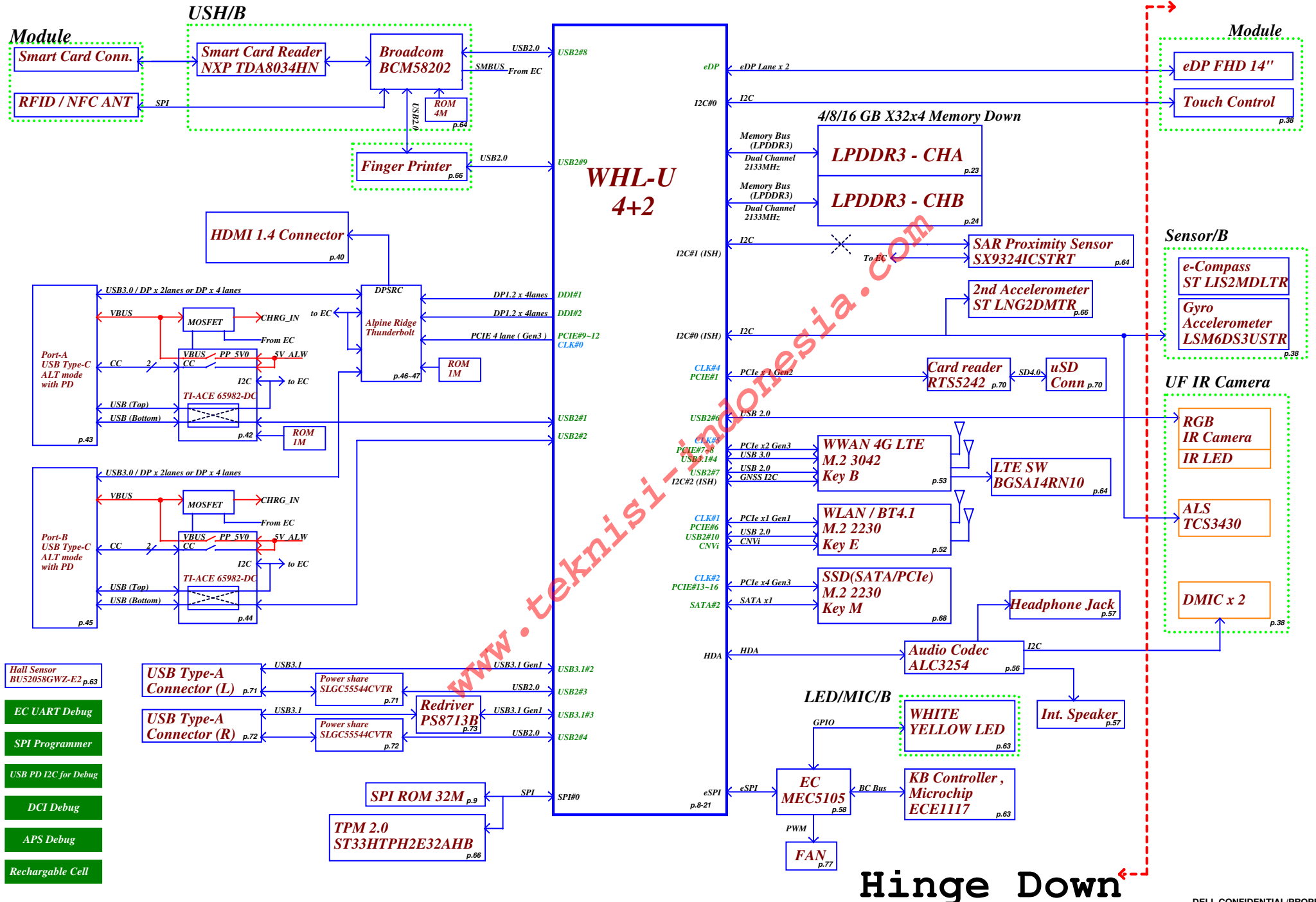
Rev: 1.0 (A00)

PVT

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Issued Date		Deciphered Date		Compal Electronics, Inc.	
2018/01/23		2022/12/31		Title	
				P001 - Cover	
				Document Number	
				LA-G441P	
				Date	
				Friday, December 14, 2018	
				Sheet	
				1 of 100	

# Hinge up



# Hinge Down

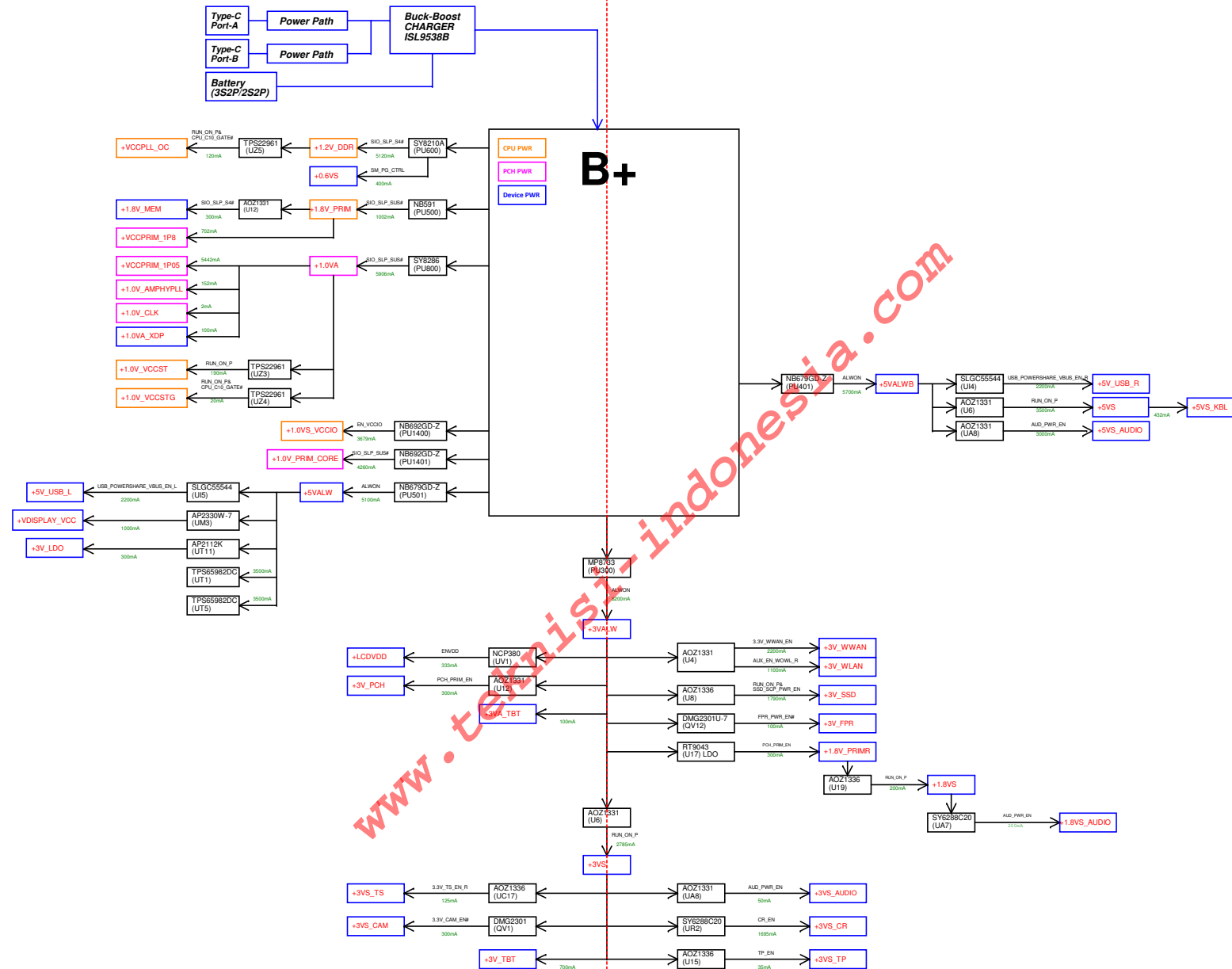
## Board ID Table

Board ID	3.3V +/- 5%	CE44	Phase	REV	PCB Revision
0	240K +/- 5%	4700p	EVT1	X00	0.1
1	130K +/- 5%	4700p	DVT1	X01	0.2
2	62K +/- 5%	4700p	DVT1.1	X02	0.3
3	33K +/- 5%	4700p	DVT2	X03	0.4
4	8.2K +/- 5%	4700p	DVT2.1	X04	0.5
5	4.3K +/- 5%	4700p	PVT	A00	1.0
6	2K +/- 5%	4700p			
7	NC				

### Board ID Option

RE200	RE200	RE200	RE200	RE200	RE200	RE200
X000	X010	X020	X030	X040	X050	X060
5C00005C0000	5C00113C000	5C00805C000	5C00C5C000	5C000000000	5C000000000	5C000000000
240K, 0402, 5%	130K, 0402, 5%	62K, 0402, 5%	33K, 0402, 5%	8.2K, 0402, 5%	8.2K, 0402, 5%	4.3K, 0602, 5%

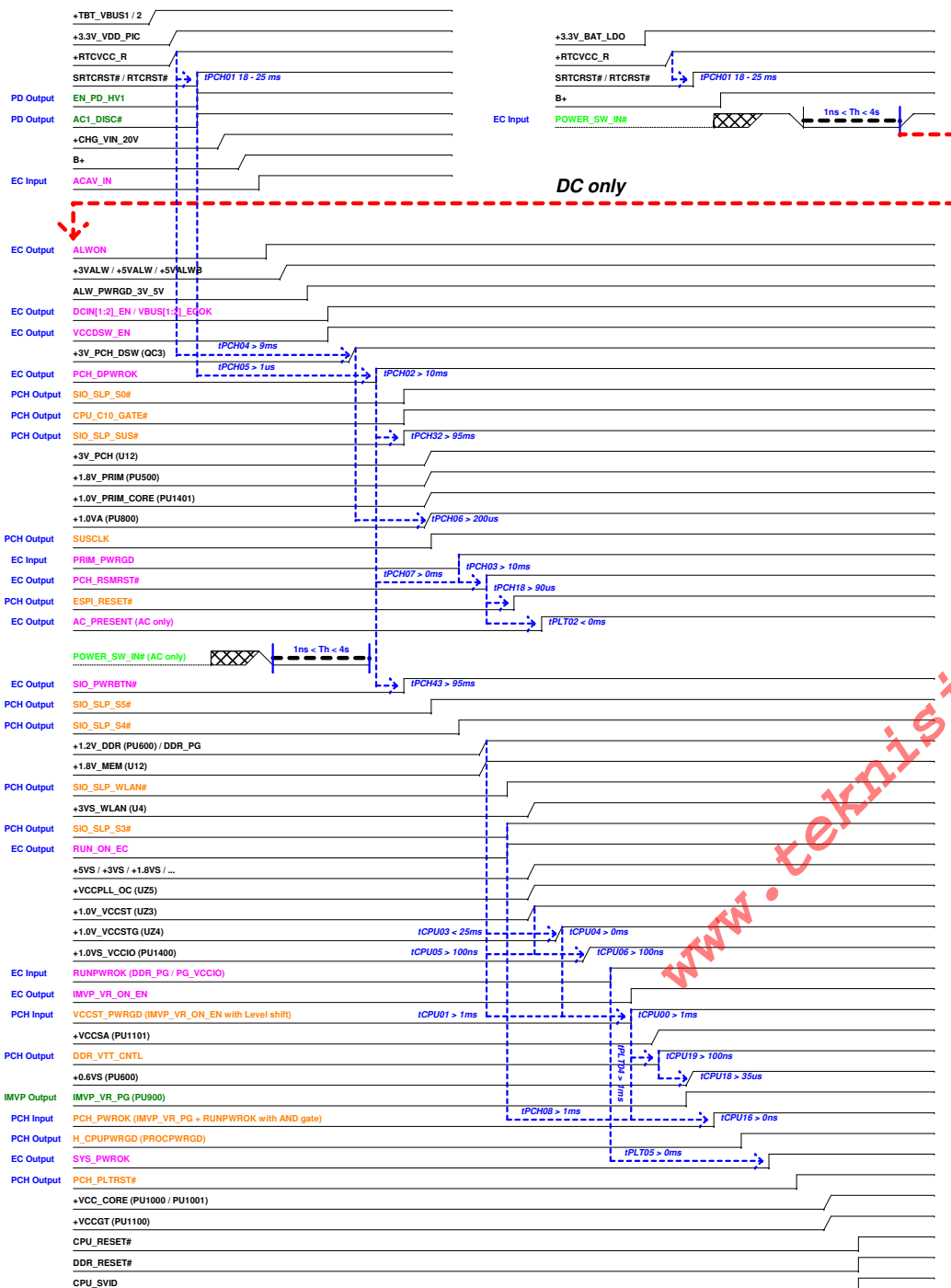
➤ **Right Side**



## Support Deep Sleep

[AC in] (remove RTC)

[Battery only, AC absent] (remove RTC)



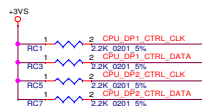
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Issued Date		Deciphered Date		11a <b>P005 - Power Sequence</b> 11b Document Number: <b>LA-G41P</b> 11c Part Number: <b>LA-G41P</b> 11d Revision: <b>001</b>	
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All VREF traces should have 10 mil trace width

COMPENSATION PU FOR eDP  
CAD Note:  
Trace width=5 mils  
Isolation Spacing=25mil,  
Max length=100 mils.

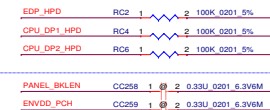
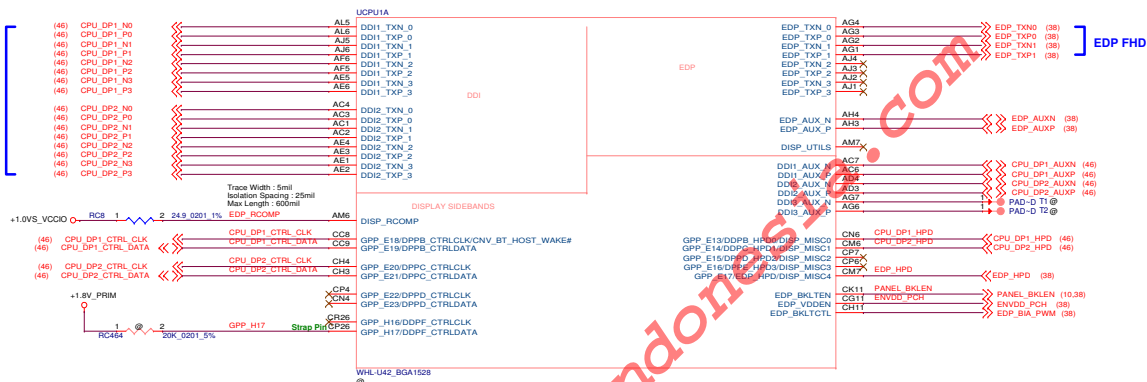


Alpine Ridge

GPP\_E19 (WEAK INTERNAL PD)  
0 = Port B is not detected. (Default)  
1 = Port B is detected.

GPP\_E21 (WEAK INTERNAL PD)  
0 = Port C is not detected. (Default)  
1 = Port C is detected.

GPP\_E23 (WEAK INTERNAL PD)  
0 = Port D is not detected. (Default)  
1 = Port D is detected.

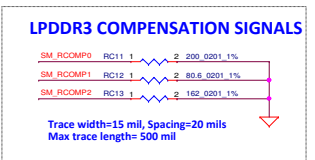
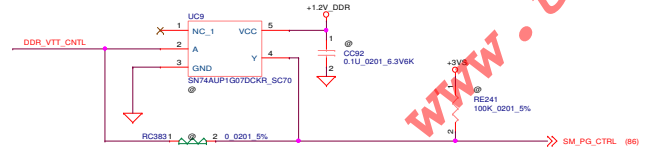
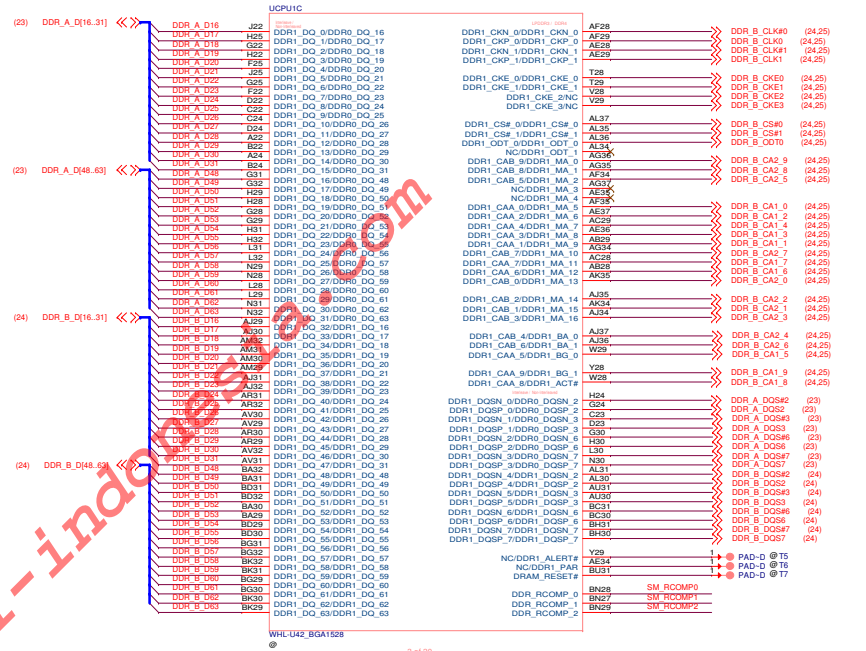
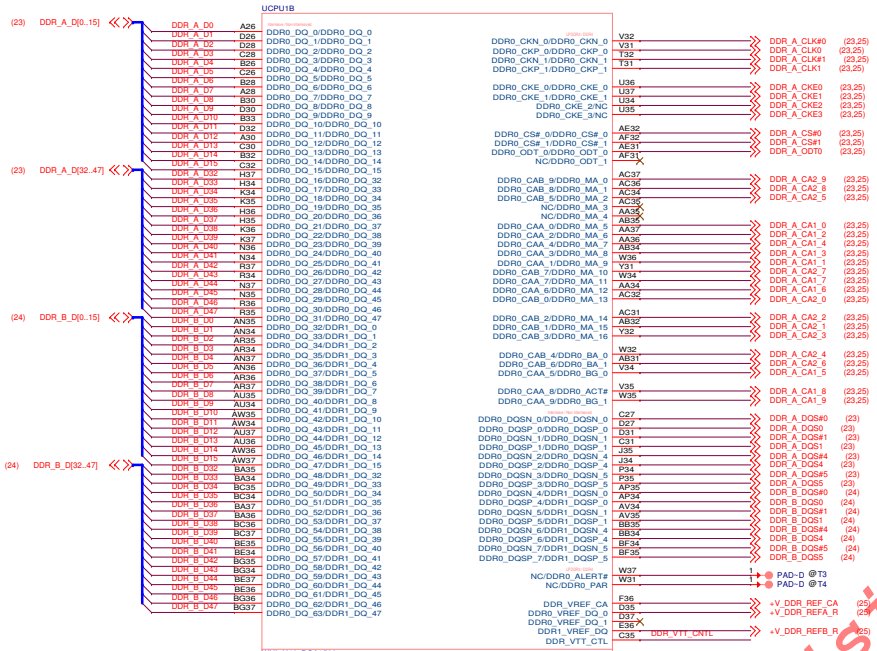


PCH GLITCH ISSUE MITIGATION(PDG p.130)

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# LPDDR3, Ballout for side by side(Non-Interleave)

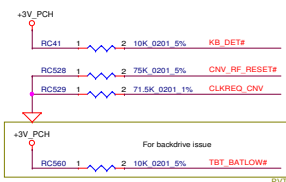






[illegible]

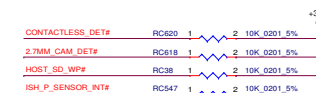
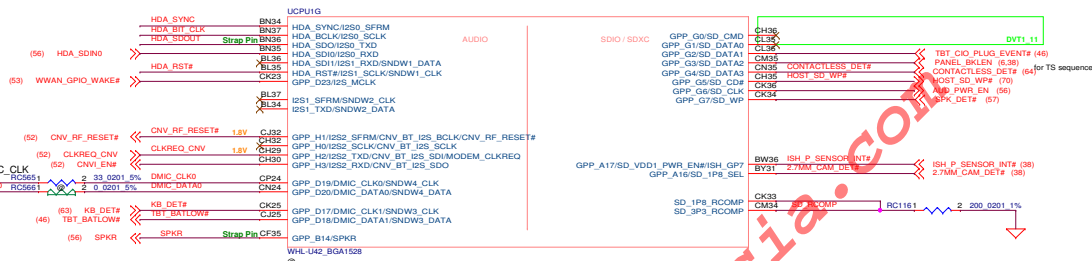
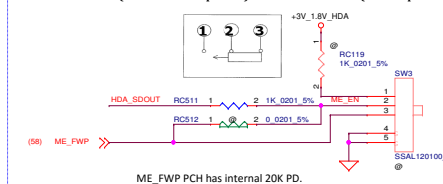
Schematic diagram of the HDA interface. It shows two signal lines: HDA\_BIT\_CLK and HDA\_RST#. HDA\_BIT\_CLK is connected to RC613 pin 1 and RC615 pin 1. HDA\_RST# is connected to RC613 pin 2 and RC615 pin 2. Both lines have a 100K 0201 5% resistor connected to ground.



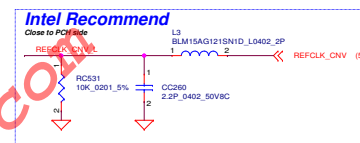
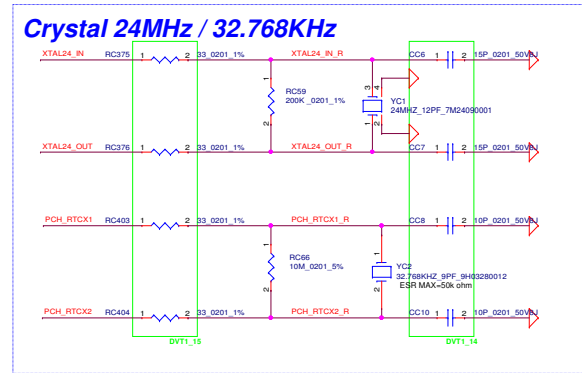
**1 = Enable Top Swap mode.**



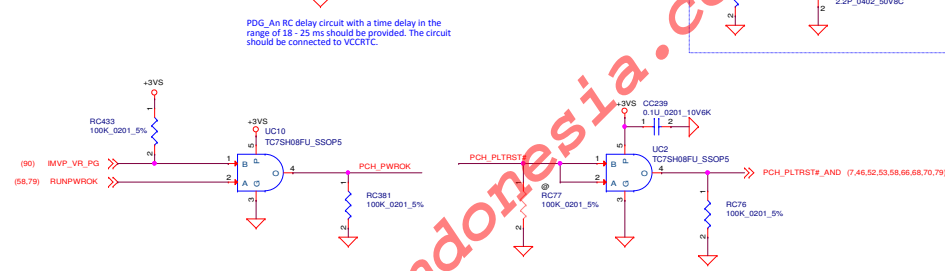
**Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default position)**



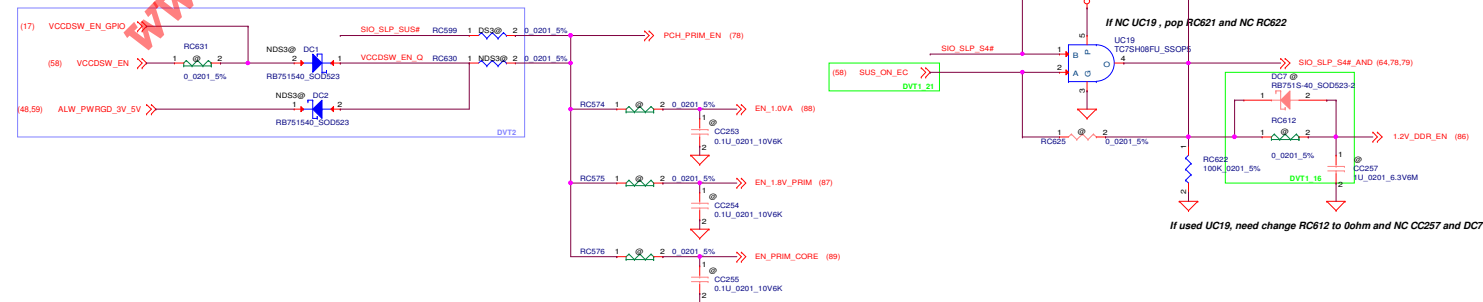
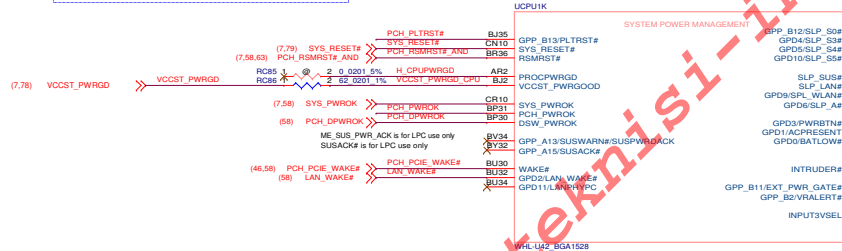
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Issued Date	2015/12/16	Deciphered Date	2016/12/13	Title <b>P010 - WHL-U(5/14)HDA,SD</b> Size Document Number <b>LA-6441P</b> Date: Friday, December 31, 2016 Sheet 10 of 100
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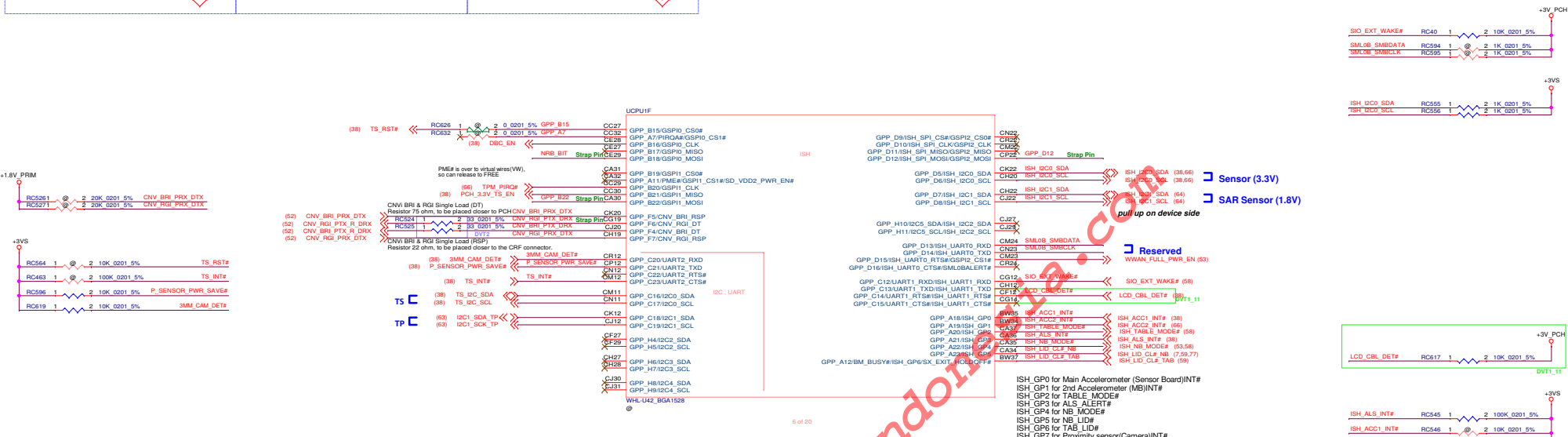
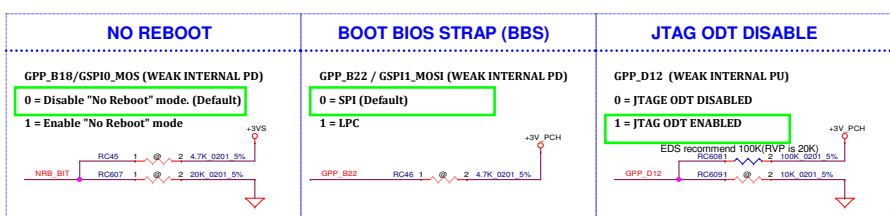


- Recommended components:
    - Ferrite bead: BLM31AG1215N1 (0201) or BLM13AG1231N1 (0402)
    - Capacitor: High frequency ceramic cap 0402 50V 1.0pF -4.7pF
- 
- Place filter components close to SOC pins (0.5 to 1mm) 201
- The following capacitor values are recommended
  - It is recommended to choose the value according to the clock trace length to account for the clock trace capacitance

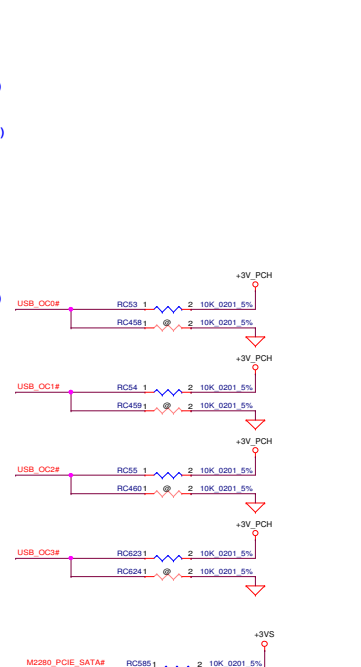
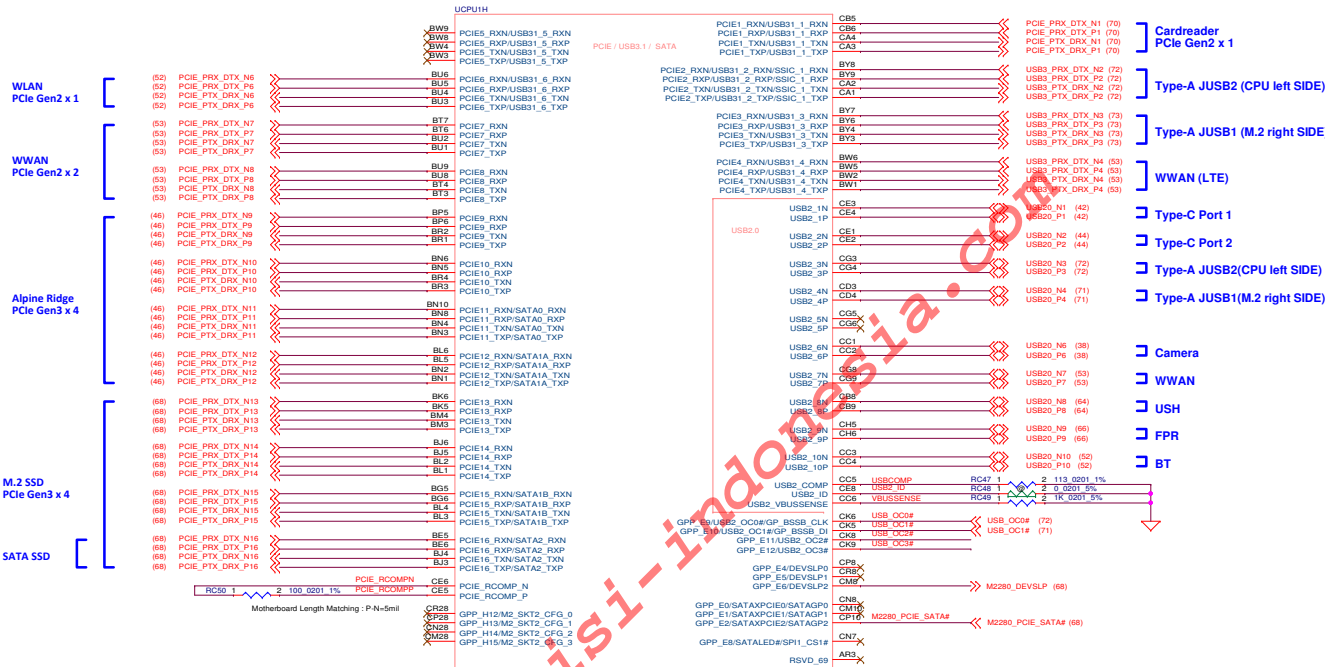


Clock route length = L	Recommended capacitor values
$L < 5"$	4.7pF
$5" < L < 9"$	2.2pF to 3.3pF
$9" < L < 10"$	1.0pF to 2.2pF





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## eSPI Flash Sharing Mode

GPP\_H23 (WEAK INTERNAL PD)

0 = MAFS enabled (Default)

1 = SAFS enabled.

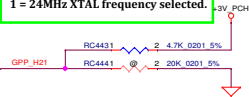


## XTAL Frequency Select

GPP\_H21 (WEAK INTERNAL PD)

0 = 38.4 XTAL frequency selected. (Default)

1 = 24MHz XTAL frequency selected.

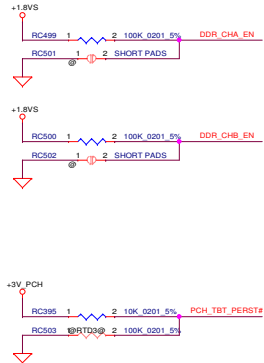


## XTAL INPUT MODE (HYM ONLY)

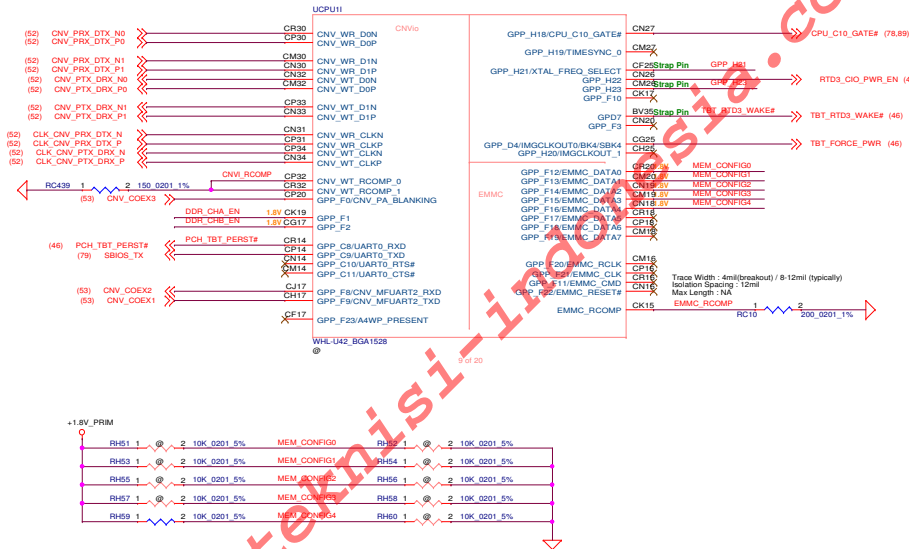
GPD7(External pull-up is required)

0 = XTAL INPUT IS SINGLE ENDED

1 = XTAL IS ATTACHED



CNV1



DDR Memory Configuration Type Strap pin

GPIO Pin	Pin Name		Micron 8Gb (4Gb)	Micron 16Gb (8Gb)	Micron 32Gb (16Gb)	Rynix 8Gb (4Gb)	Rynix 16Gb (8Gb)	Rynix 32Gb (16Gb)	Samsung 8Gb (4Gb)	Samsung 16Gb (8Gb)	Samsung 32Gb (16Gb)
GPP_F12	MEM_CONFIG0	2133 Mbps	0	1	0	1	0	1	0	1	0
GPP_F13	MEM_CONFIG1		1	1	0	0	1	1	0	0	1
GPP_F14	MEM_CONFIG2		0	0	1	1	1	1	0	0	0
GPP_F15	MEM_CONFIG3		0	0	0	0	0	0	1	1	1
GPP_F16	MEM_CONFIG4		1	1	1	1	1	1	1	1	1

DELL CONFIDENTIAL/PROPRIETARY

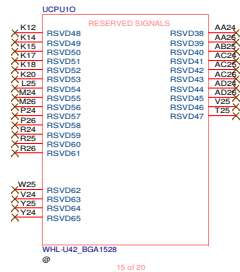
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P014 - WHL-U(9/14)CNV,EMMC

LA-G441P

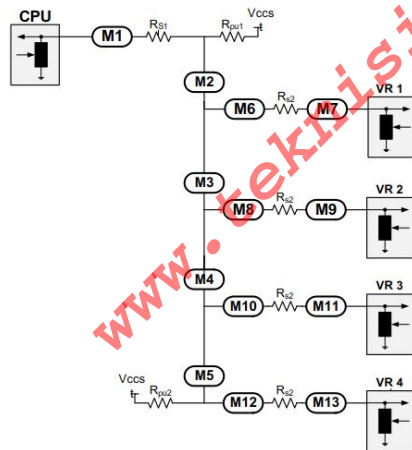
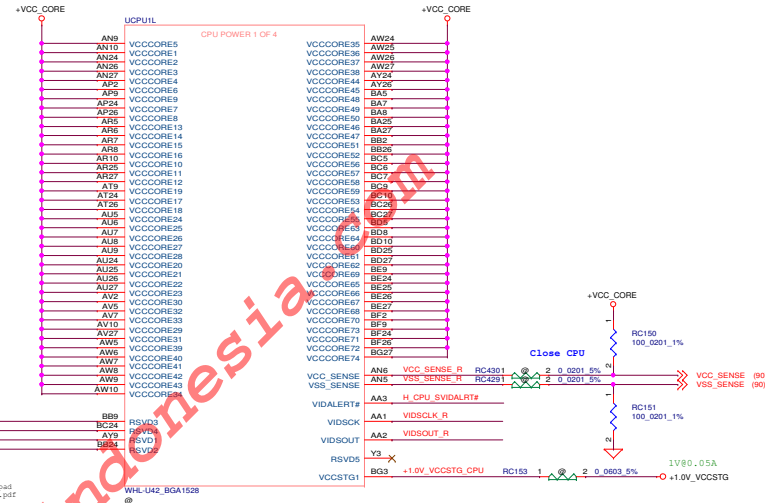
Pin Number	CTL Data	WHL U42 Q6/Production	ICN U42/WHL U42 ESD1
AV28	21W	RSVD	RSVD
T25	VCCOPD_SENSE	RSVD	RSVD
V25	VCCOPD_SENSE	RSVD	RSVD
AA34	VCCOPD	RSVD	RSVD
AA36	VCCOPD	RSVD	RSVD
AA38	VCCOPD	RSVD	RSVD
AA39	VCCOPD	RSVD	RSVD
AA40	VCCOPD	RSVD	RSVD
AA41	VCCOPD	RSVD	RSVD
AA42	VCCOPD	RSVD	RSVD
AA43	VCCOPD	RSVD	RSVD
AA44	VCCOPD	RSVD	RSVD
AA45	VCCOPD	RSVD	RSVD
AA46	VCCOPD	RSVD	RSVD
AA47	VCCOPD	RSVD	RSVD
AA48	VCCOPD	RSVD	RSVD
AA49	VCCOPD	RSVD	RSVD
AA50	VCCOPD	RSVD	RSVD
AA51	VCCOPD	RSVD	RSVD
AA52	VCCOPD	RSVD	RSVD
AA53	VCCOPD	RSVD	RSVD
AA54	VCCOPD	RSVD	RSVD
AA55	VCCOPD	RSVD	RSVD
AA56	VCCOPD	RSVD	RSVD
AA57	VCCOPD	RSVD	RSVD
AA58	VCCOPD	RSVD	RSVD
AA59	VCCOPD	RSVD	RSVD
AA60	VCCOPD	RSVD	RSVD
AA61	VCCOPD	RSVD	RSVD
AA62	VCCOPD	RSVD	RSVD
AA63	VCCOPD	RSVD	RSVD
AA64	VCCOPD	RSVD	RSVD
AA65	VCCOPD	RSVD	RSVD
AA66	VCCOPD	RSVD	RSVD
AA67	VCCOPD	RSVD	RSVD
AA68	VCCOPD	RSVD	RSVD
AA69	VCCOPD	RSVD	RSVD
AA70	VCCOPD	RSVD	RSVD
AA71	VCCOPD	RSVD	RSVD
AA72	VCCOPD	RSVD	RSVD
AA73	VCCOPD	RSVD	RSVD
AA74	VCCOPD	RSVD	RSVD
AA75	VCCOPD	RSVD	RSVD
AA76	VCCOPD	RSVD	RSVD
AA77	VCCOPD	RSVD	RSVD
AA78	VCCOPD	RSVD	RSVD
AA79	VCCOPD	RSVD	RSVD
AA80	VCCOPD	RSVD	RSVD
AA81	VCCOPD	RSVD	RSVD
AA82	VCCOPD	RSVD	RSVD
AA83	VCCOPD	RSVD	RSVD
AA84	VCCOPD	RSVD	RSVD
AA85	VCCOPD	RSVD	RSVD
AA86	VCCOPD	RSVD	RSVD
AA87	VCCOPD	RSVD	RSVD
AA88	VCCOPD	RSVD	RSVD
AA89	VCCOPD	RSVD	RSVD
AA90	VCCOPD	RSVD	RSVD
AA91	VCCOPD	RSVD	RSVD
AA92	VCCOPD	RSVD	RSVD
AA93	VCCOPD	RSVD	RSVD
AA94	VCCOPD	RSVD	RSVD
AA95	VCCOPD	RSVD	RSVD
AA96	VCCOPD	RSVD	RSVD
AA97	VCCOPD	RSVD	RSVD
AA98	VCCOPD	RSVD	RSVD
AA99	VCCOPD	RSVD	RSVD
AA100	VCCOPD	RSVD	RSVD



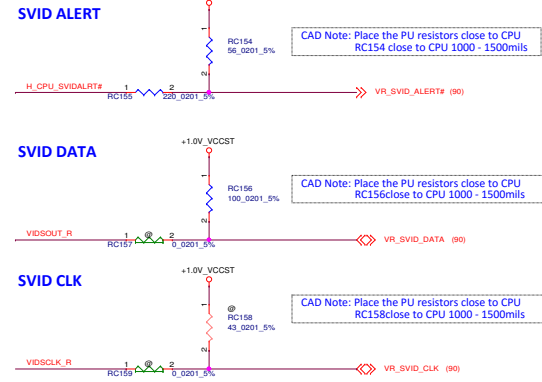
PSC(Primary side cap) : Place as close to the package as possible  
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:  
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

+VCC\_CORE: 0.55~1.5V, 29A  
+VCC\_EDRAM: 1V, 2.5A  
+V1.8S\_EDRAM: 1.8V, 50mA - REMOVE  
+VCC\_EOPIO: 0.8~1V, 2A - REMOVE



VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω

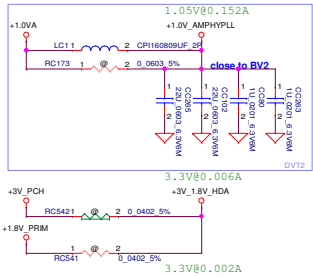


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			Sheet	16 of 100

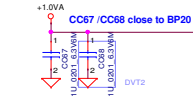


VCCA\_1P2\_1P05 : 0.027A  
VCCAPLL\_1P05 : 0.102A  
VCCA\_BCLK\_1P05 : 0.009A  
VCCA\_SEC\_1P05 : 0.042A  
VCCPRIM\_1P05 : 1.625A  
VCCDUSB\_1P05 : 0.28A  
VCCDSW\_1P05 : 0.024A  
VCCPRIM\_MPHY\_1P05 : 3.333A  
USB3.1(10 Gb/s) : 0.259\*3 port = 0.777A  
PCIe(Gen3) : 0.213\*12 port = 2.556A

PDG: 1U\_0402\*1 + 47U\_0603\*1 + 2.2uH inductor



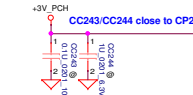
1.05V85\_442A



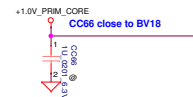
1.8V80\_702A



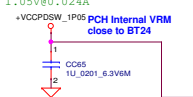
3.3V80\_199A



1.05V84\_26A



1.05V80\_024A



1.05V80\_006A



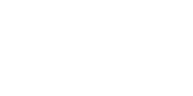
1.05V80\_002A



1.05V80\_001A



1.05V80\_000A



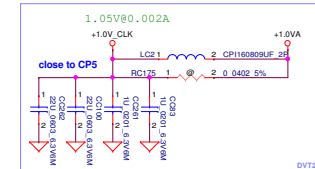
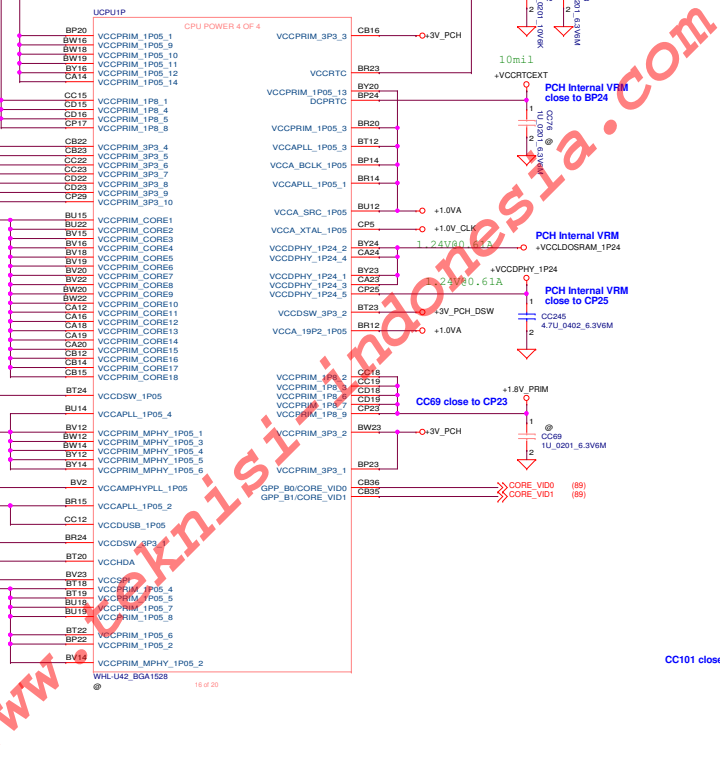
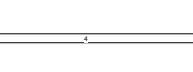
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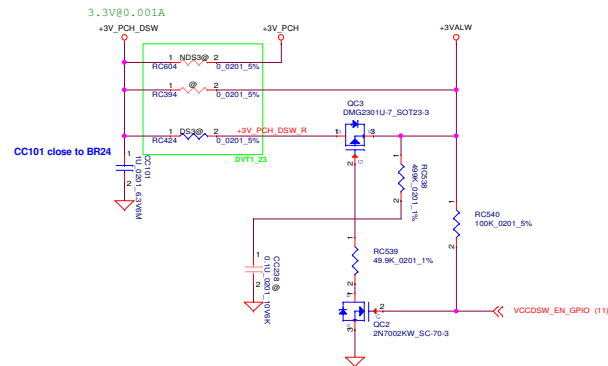
1.05V80\_000A



1.05V80\_000A



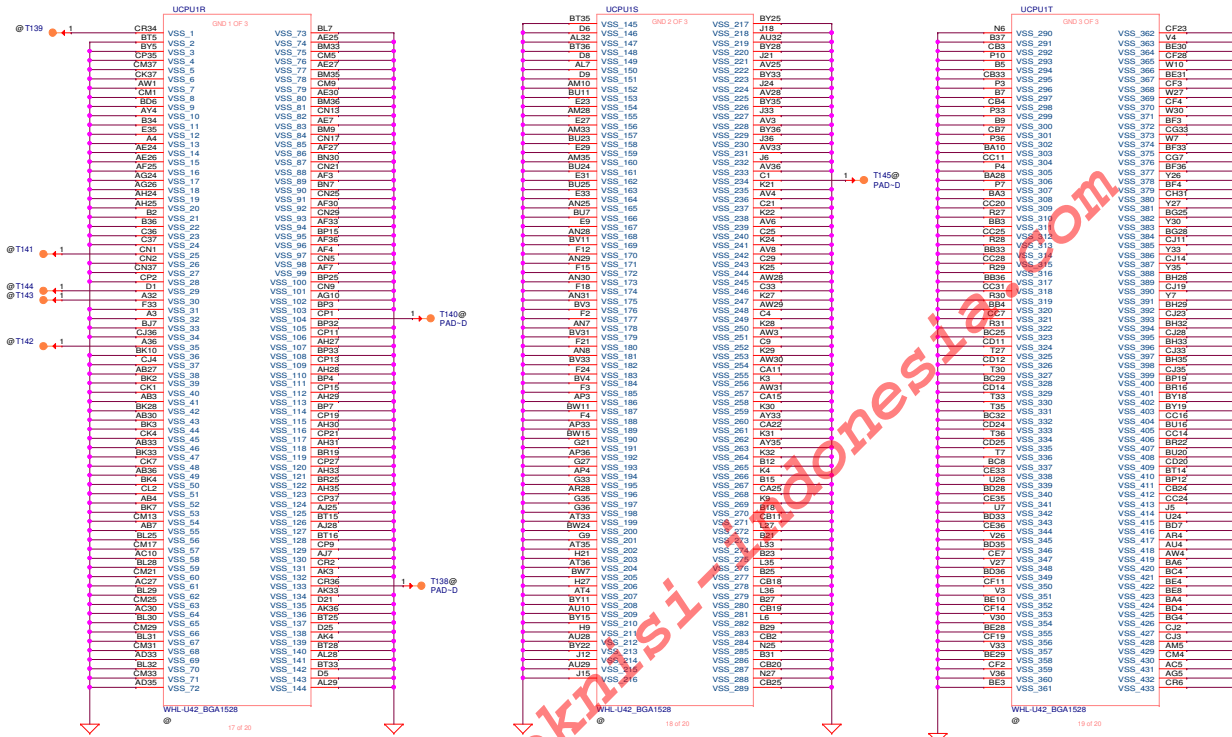
PDG: 1U\_0402\*1 + 47U\_0603\*1 + 2.2uH inductor

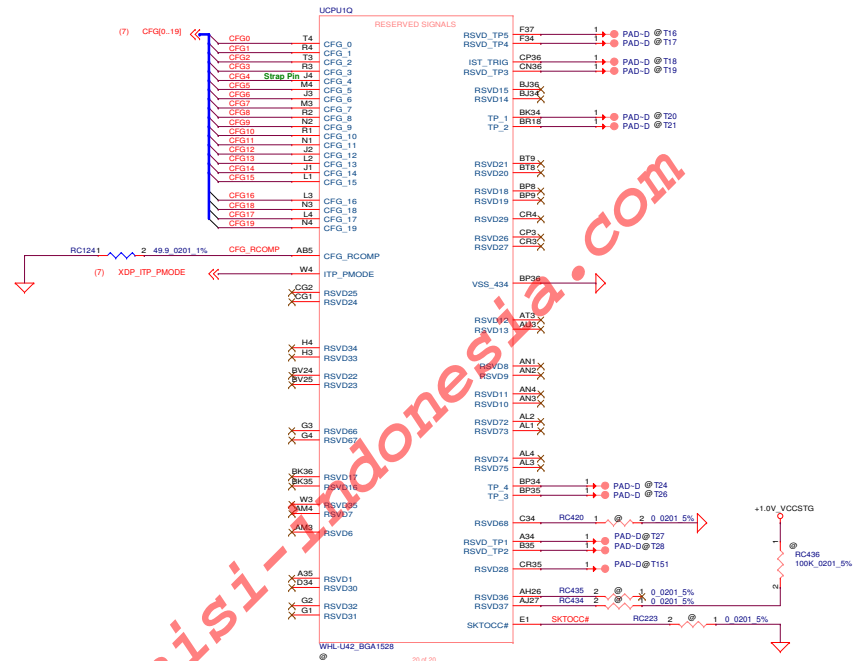
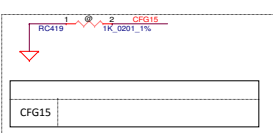
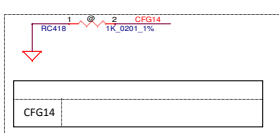
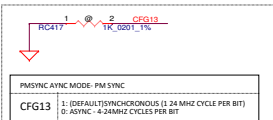
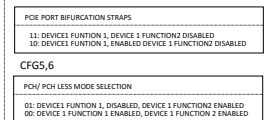
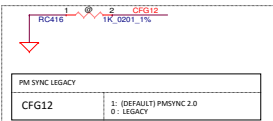
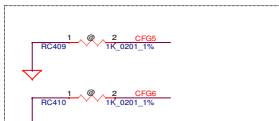
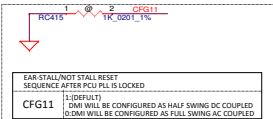
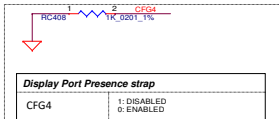
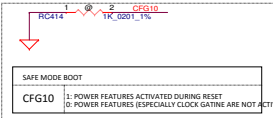
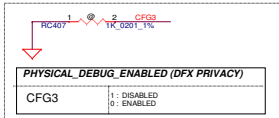
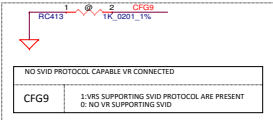
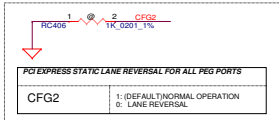
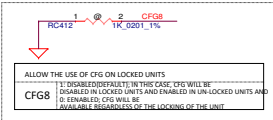
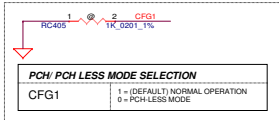
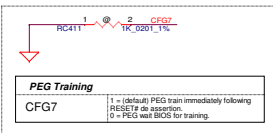
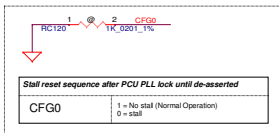


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Date:		Friday, December 14, 2016		Sheet 17 of 100	

Test pin for Corner NCTF Test(#566757)  
need place on CPU corner

Note1: VCCPRIM\_CORE Implementation with PCH CORE\_VID Recommendation





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				Date	Rev
				Friday, December 14, 2018	0.1(X00)
				Sheet 20 of 100	

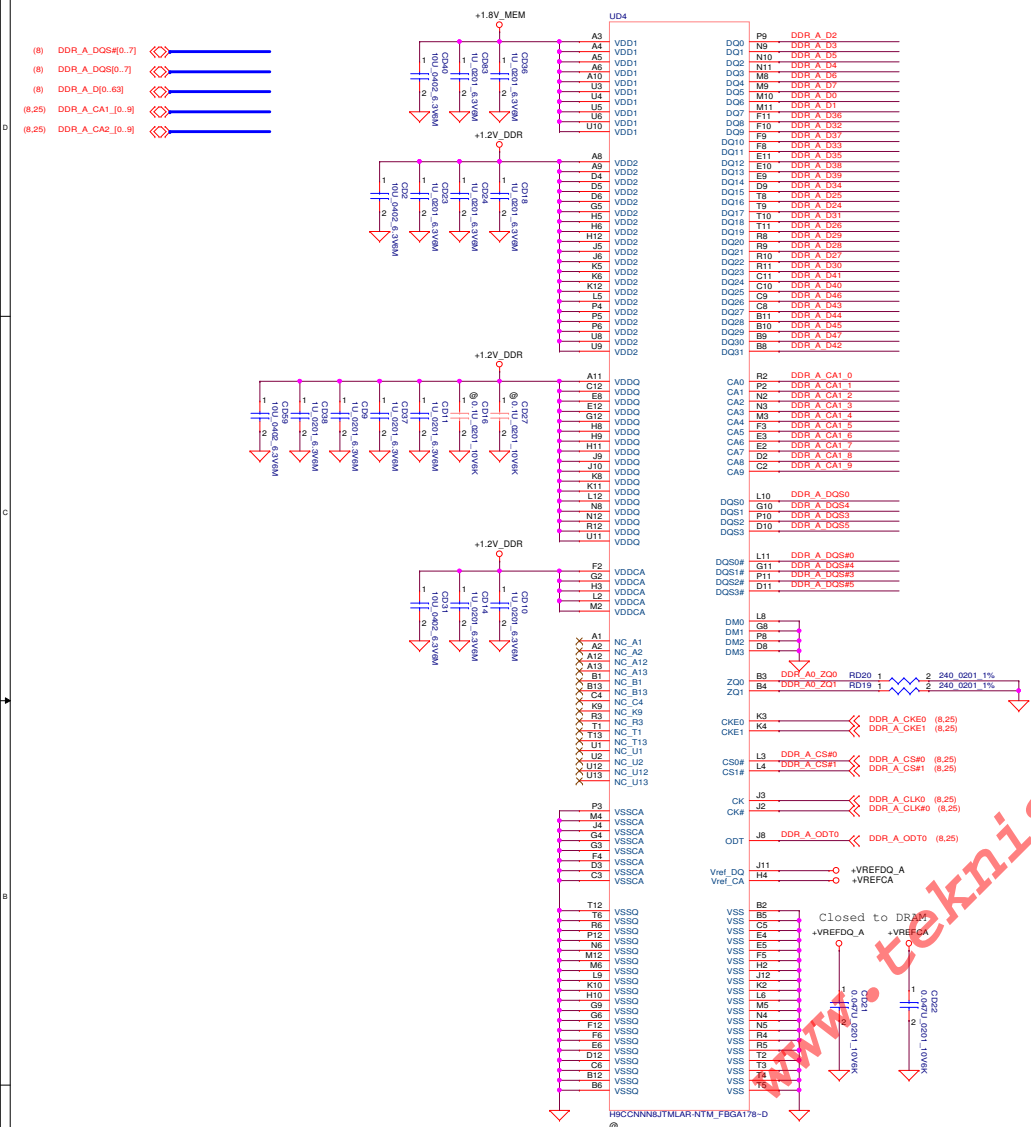
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				Date: Friday, December 14, 2018	Sheet 21 of 100
				Rev	0.1(X00)

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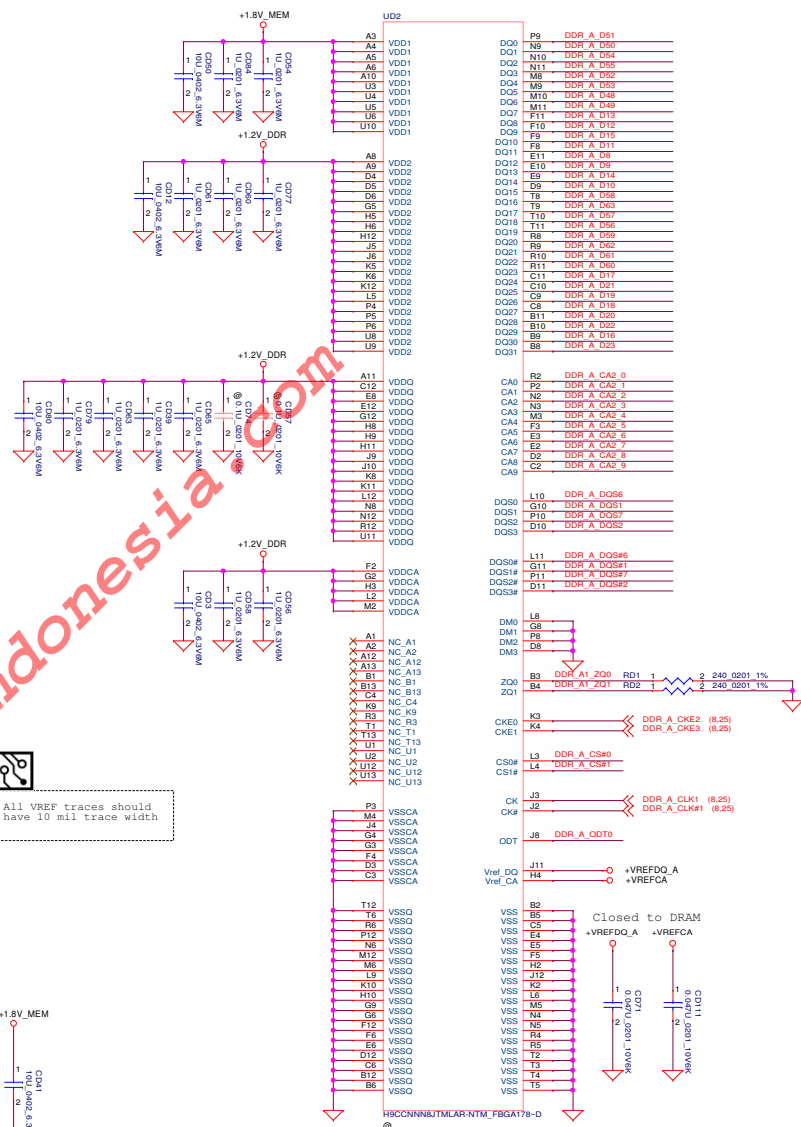
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Date: Friday, December 14, 2018				Sheet	22 of 100

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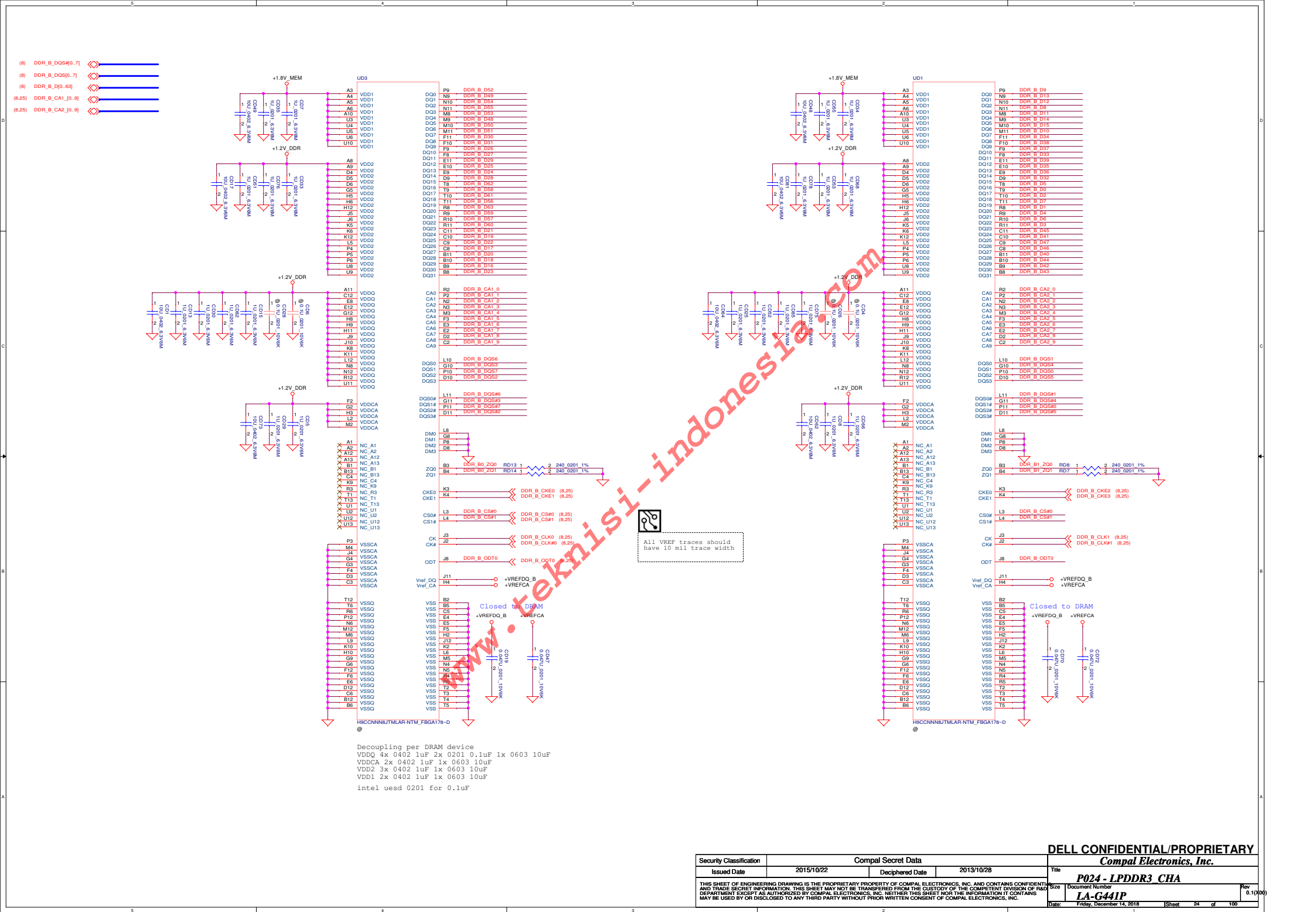


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Decoupling per DRAM device
VDDQ 4x 0402 1uF 2x 0201 0.1uF 1x 0603 10uF
VDDCA 2x 0402 1uF 1x 0603 10uF
VDD2 3x 0402 1uF 1x 0603 10uF
VDD1 2x 0402 1uF 1x 0603 10uF

intel used 0201 for 0.1uF
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				Date:	Friday, December 14, 2018 <div style="float: right;">           Sheet 23 of 100         </div>



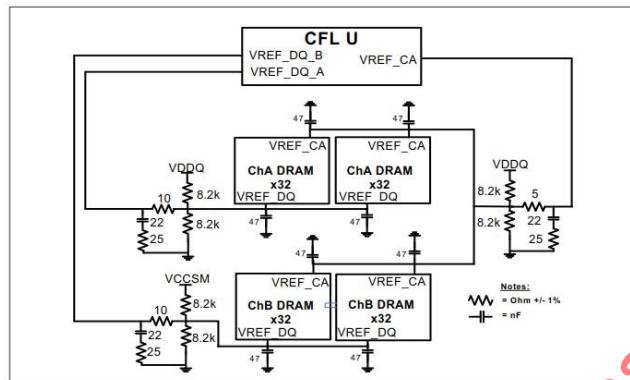
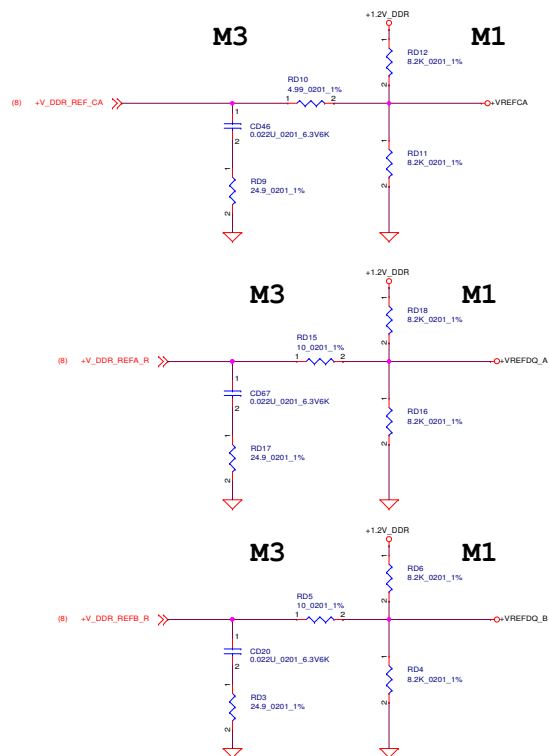
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VDD1 2x 0402 1uF 1x 0603 10uF  
intel used 0201 for 0.1uF

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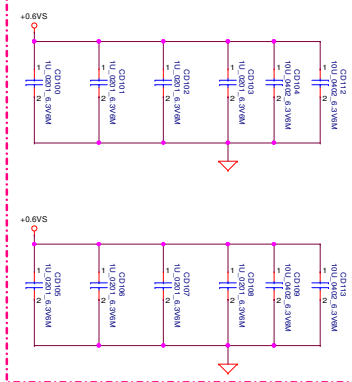




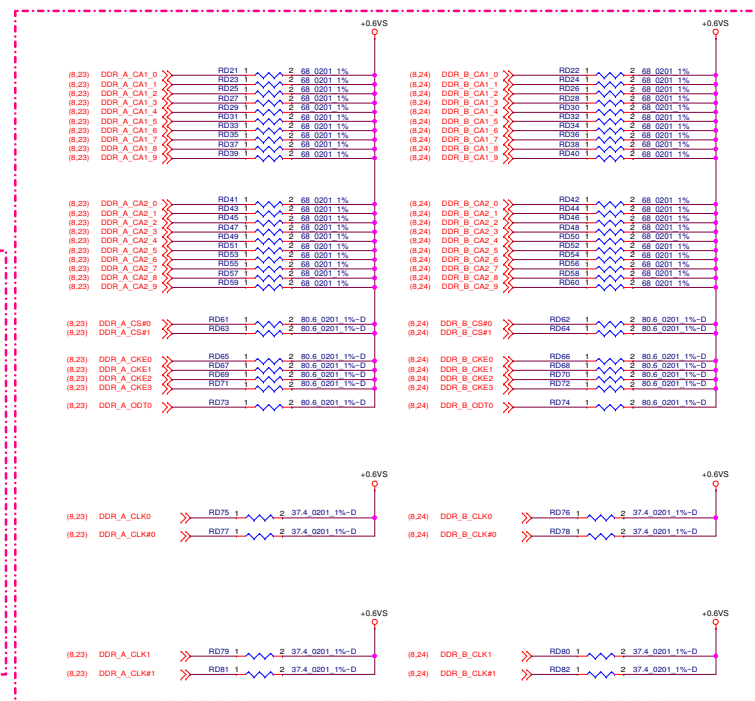
VREF traces should be at least 20 mils wide with 20 mils spacing to other signals/planes.



Add for RAM RTD function



Add for RAM RTD function



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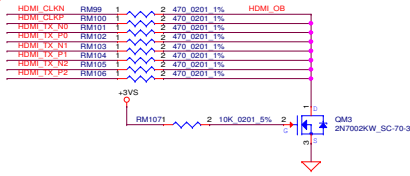
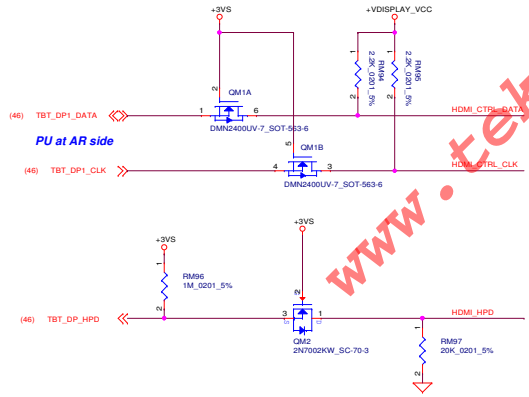
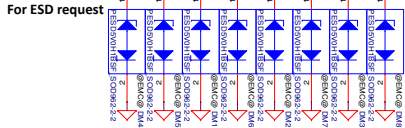
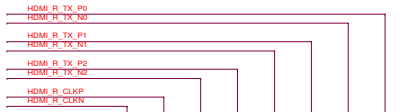
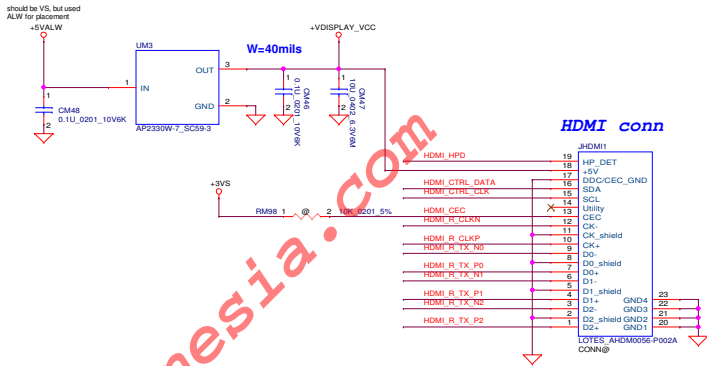
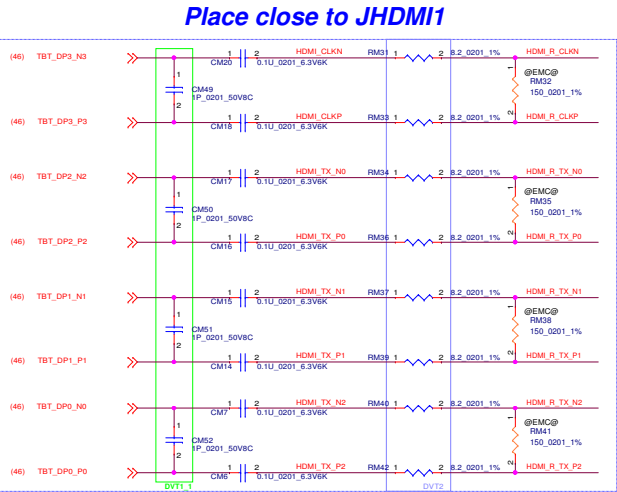
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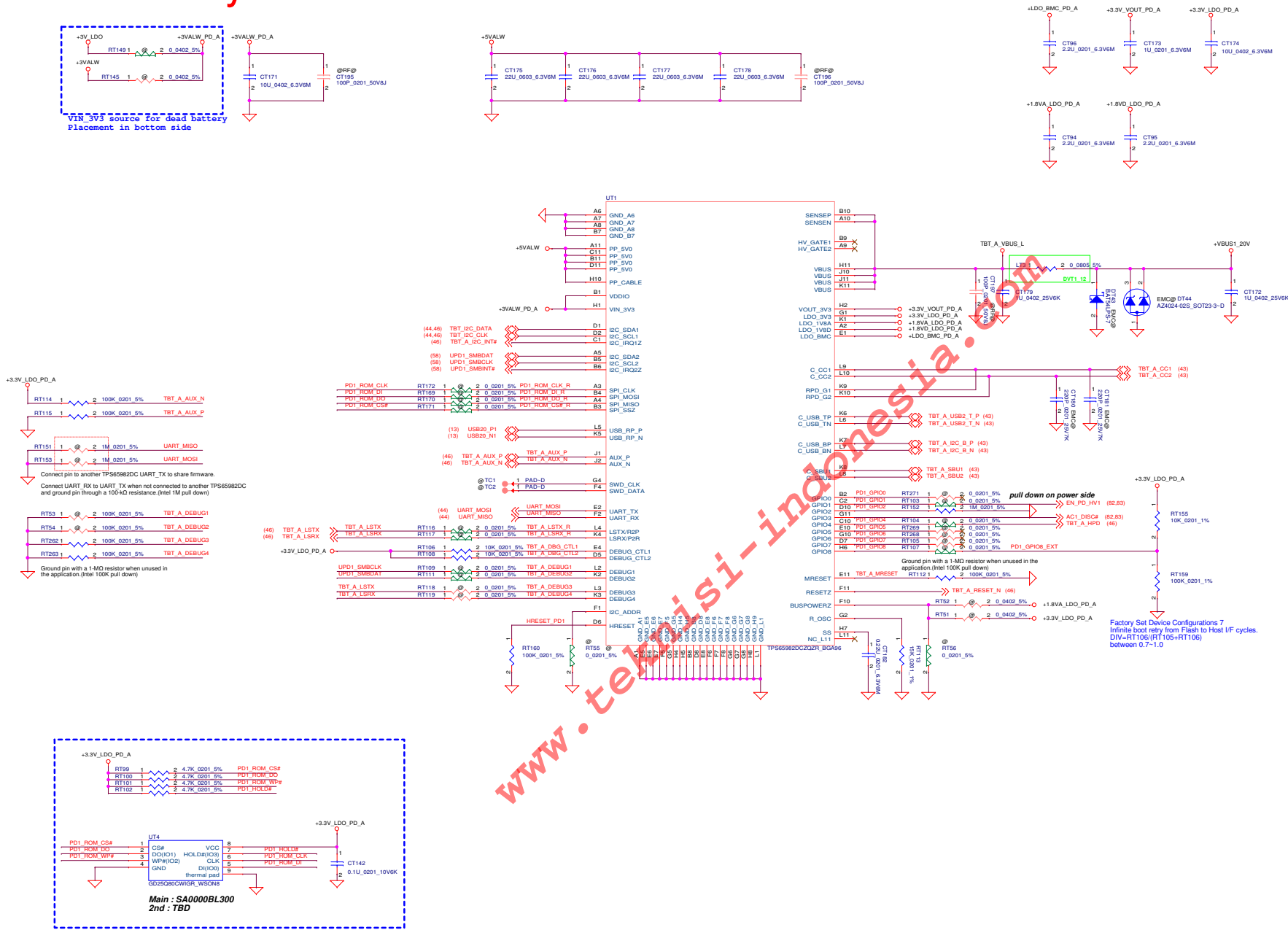




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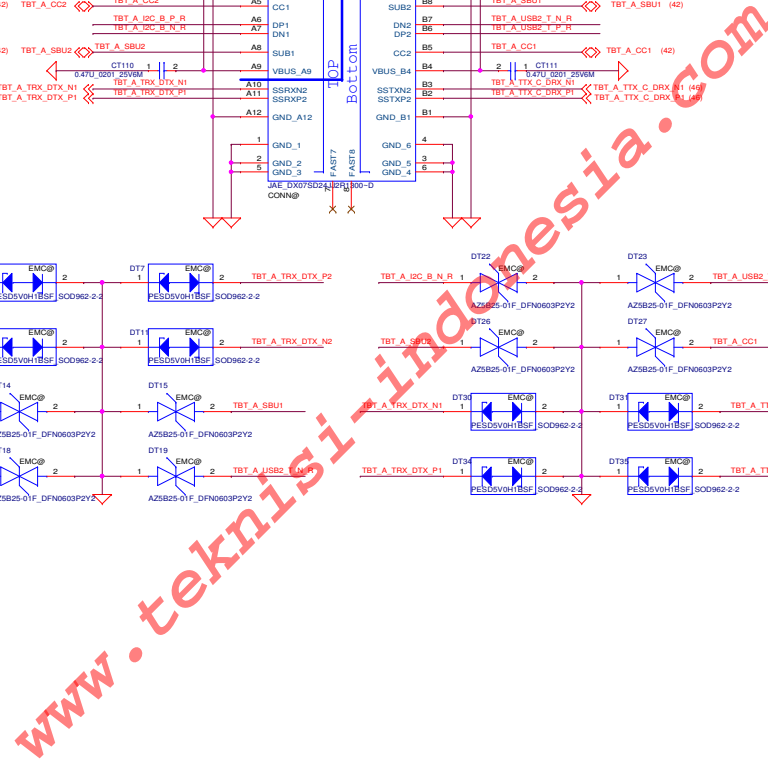
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**USB Type-C Receptacle Interface (Front View)**

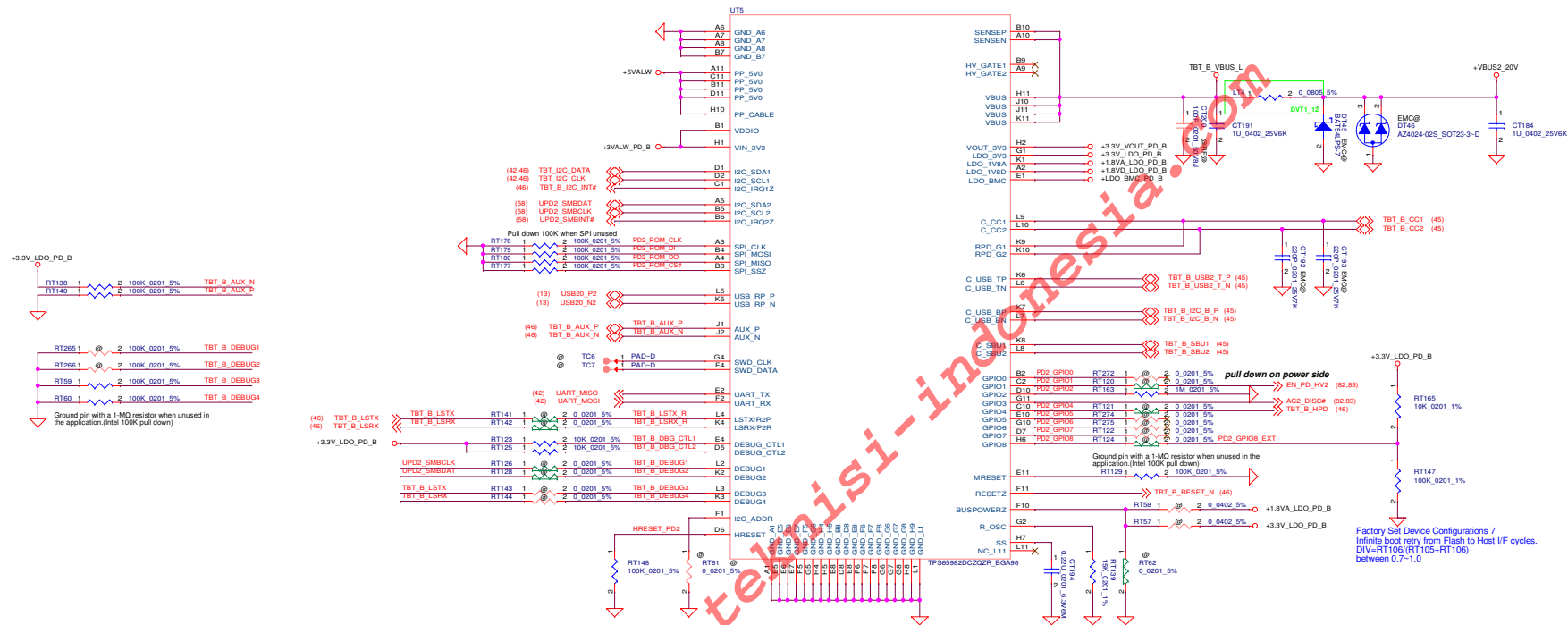
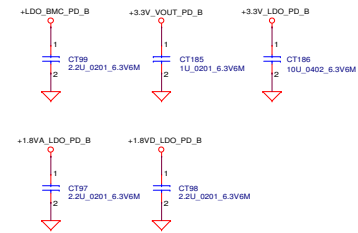
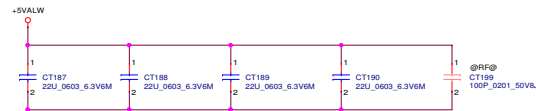
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	A3	A10	
	A4	A9	
	A5	A8	
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	A7	A6	
	A8	A5	
	A9	A4	
	A10	A3	
	A11	A2	
	A12	A1	
	GND		
	TX1+		
	TX1-		
	VBUS		
	CC1		
	D+		
	D-		
	SBU1		
	VBUS		
	RX2-		
	RX2+		
	GND		
	GND		
	RX1+		
	RX1-		
	VBUS		
	SBU2		
	D-		
	D+		
	CC2		
	VBUS		
	TX2-		
	TX2+		
	GND		
	B12		
	B11		
	B10		
	B9		
	B8		
	B7		
	B6		
	B5		
	B4		
	B3		
	B2		
	B1		
Pin24			Pin13

**Printed Circuit Board**



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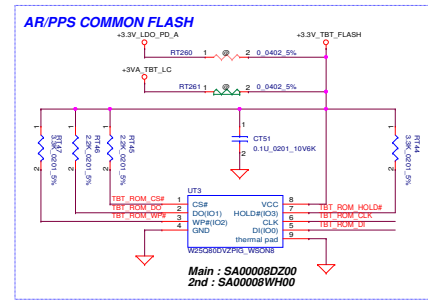
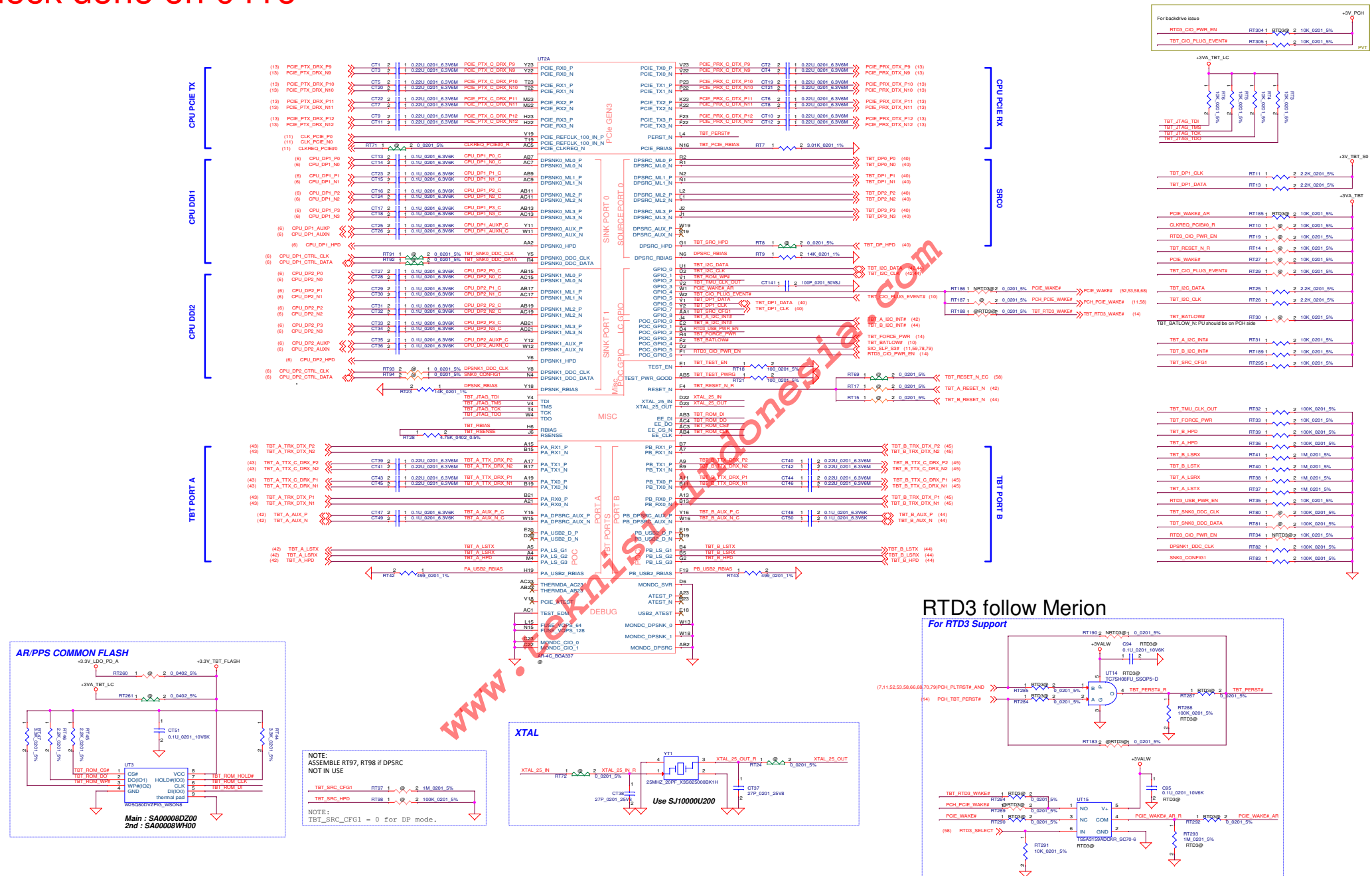
VIN\_3V3 source for dead battery  
Placement in bottom side



Factory Set Device Configurations 7  
Infinite boot retry from Flash to Host I/F cycles  
 $DIV = RT106 / (RT105 + RT106)$   
between 0.7~1.0



Check done on 0416



NOTE:  
ASSEMBLE RT97, RT98 if DPSRC  
NOT IN USE

NOTE:  
TBT\_SRC\_CFG1 = 0 for DP mode.

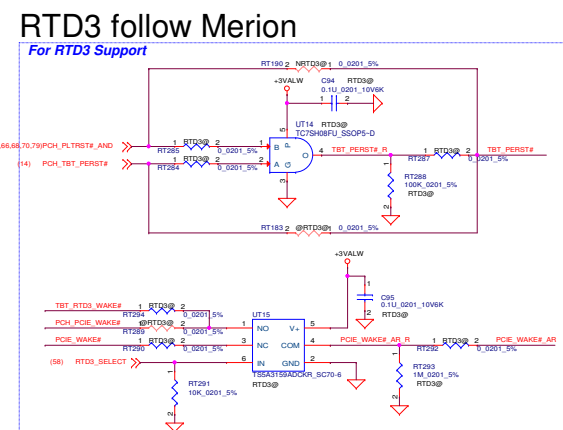
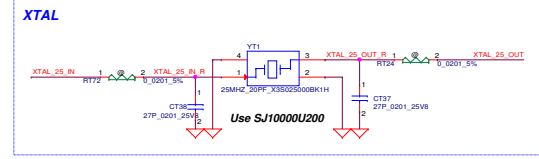
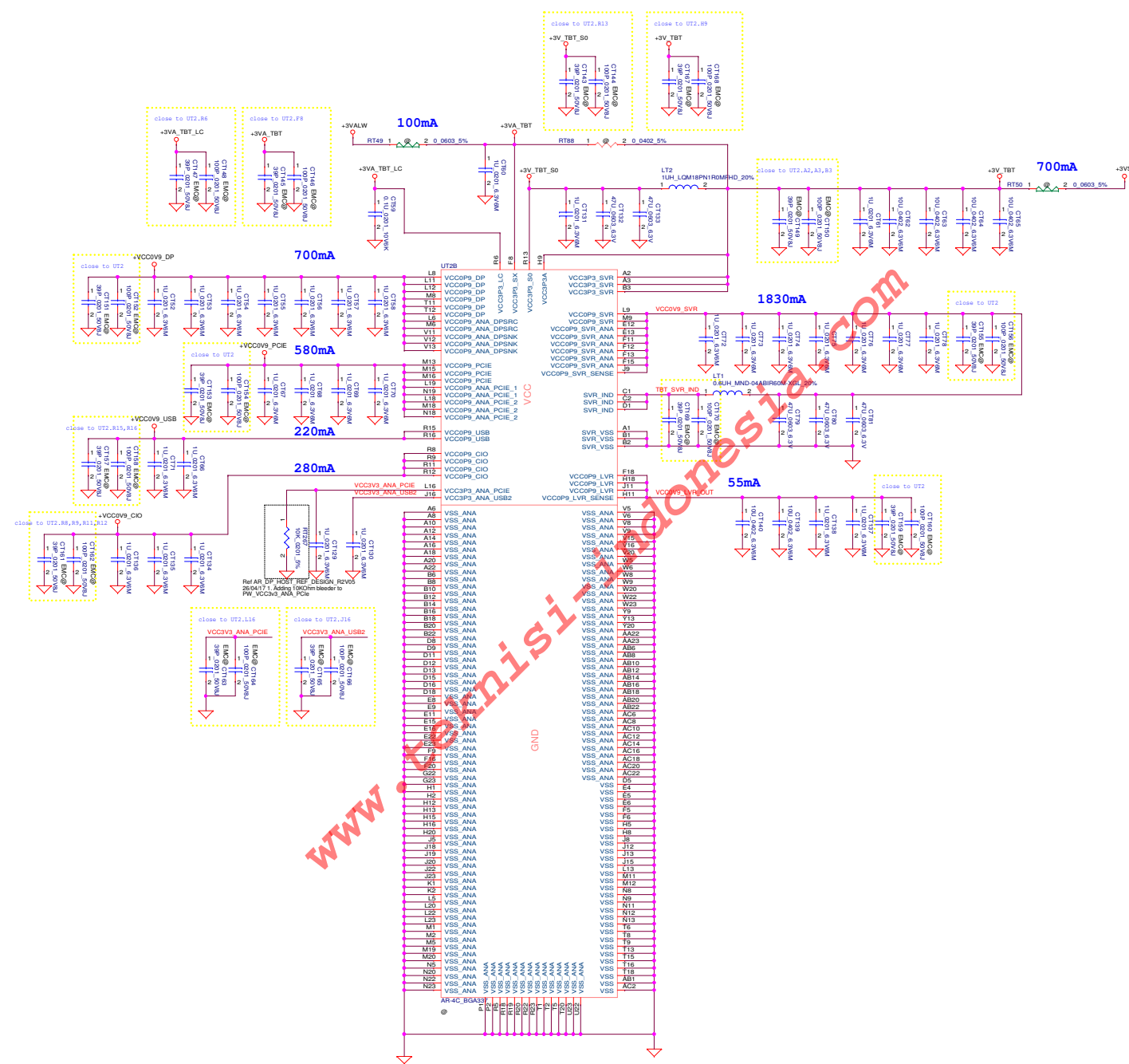


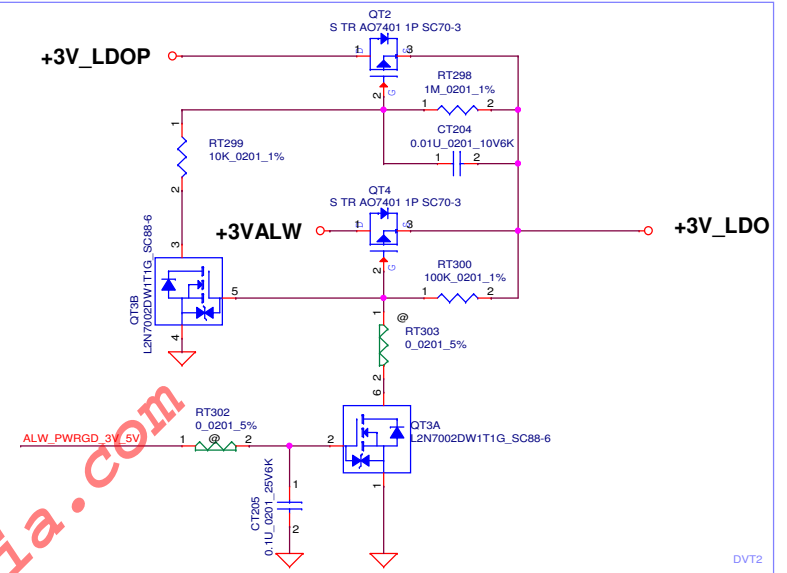
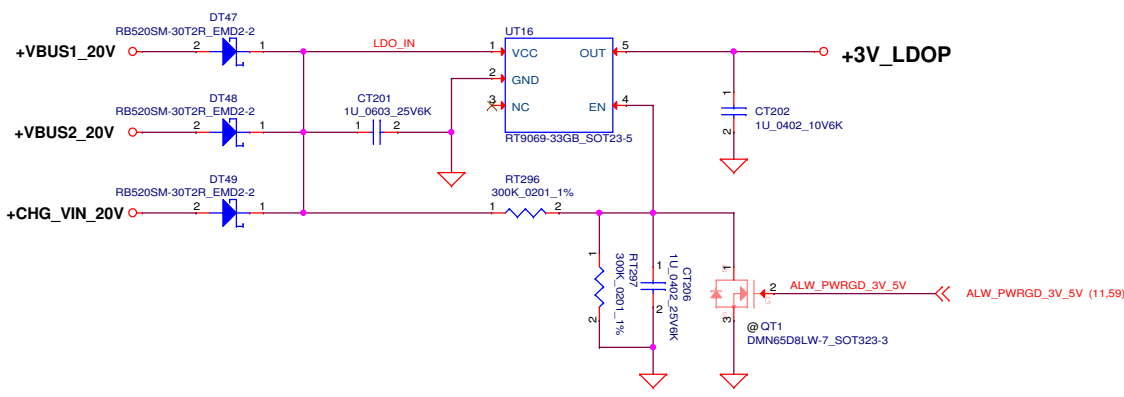
Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

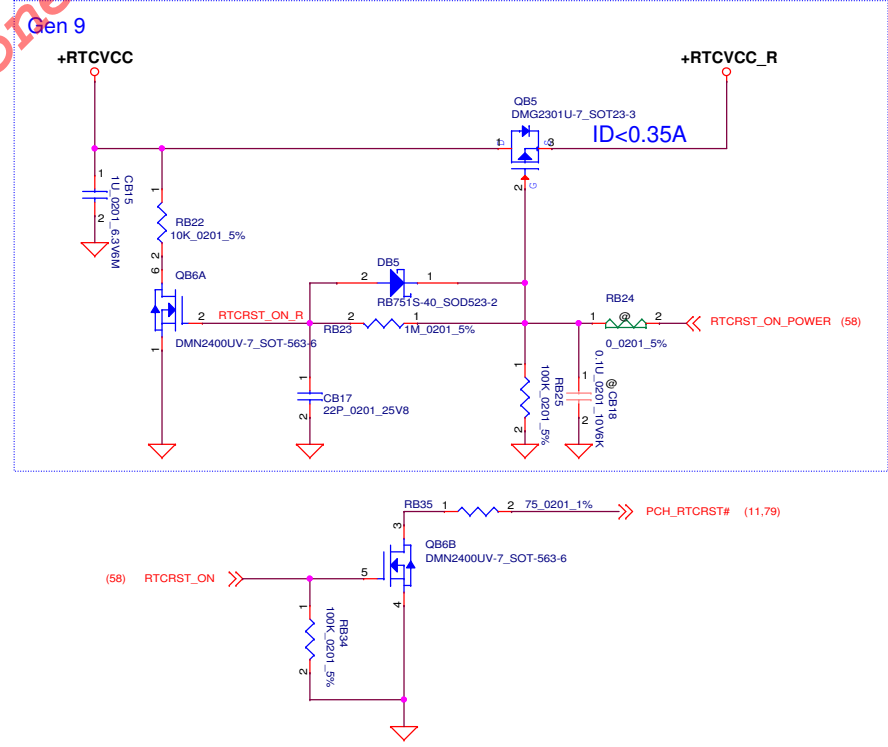
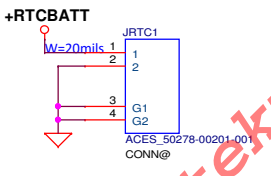
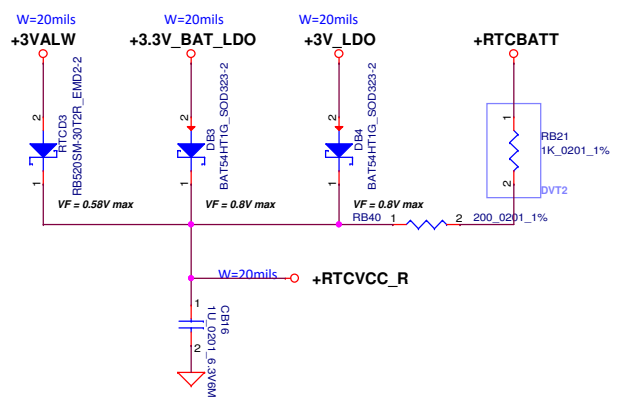
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# 3V\_LDO power



# RTC



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				Sheet 50 of 100	

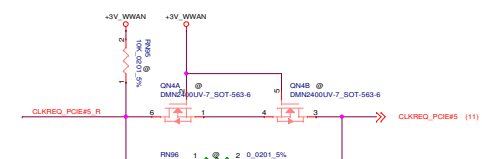
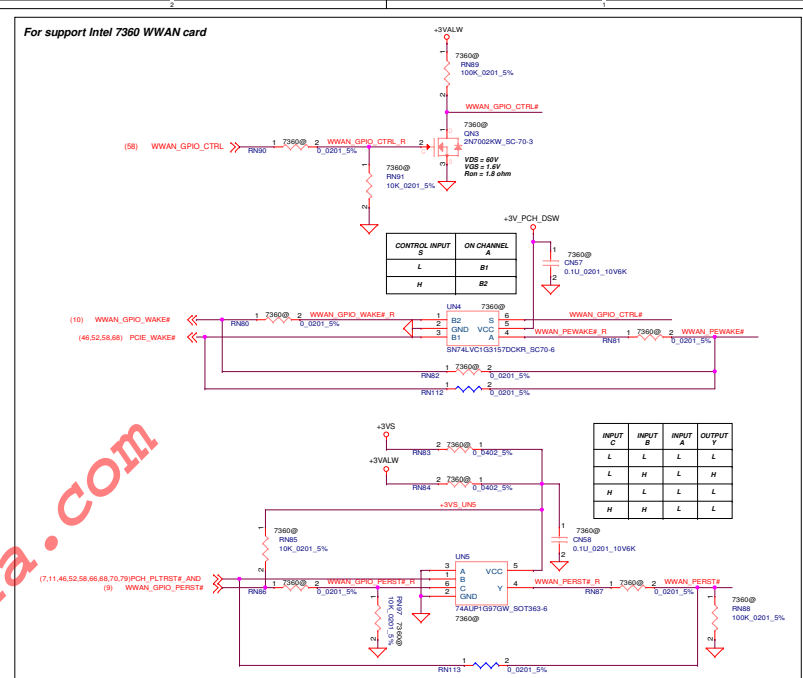
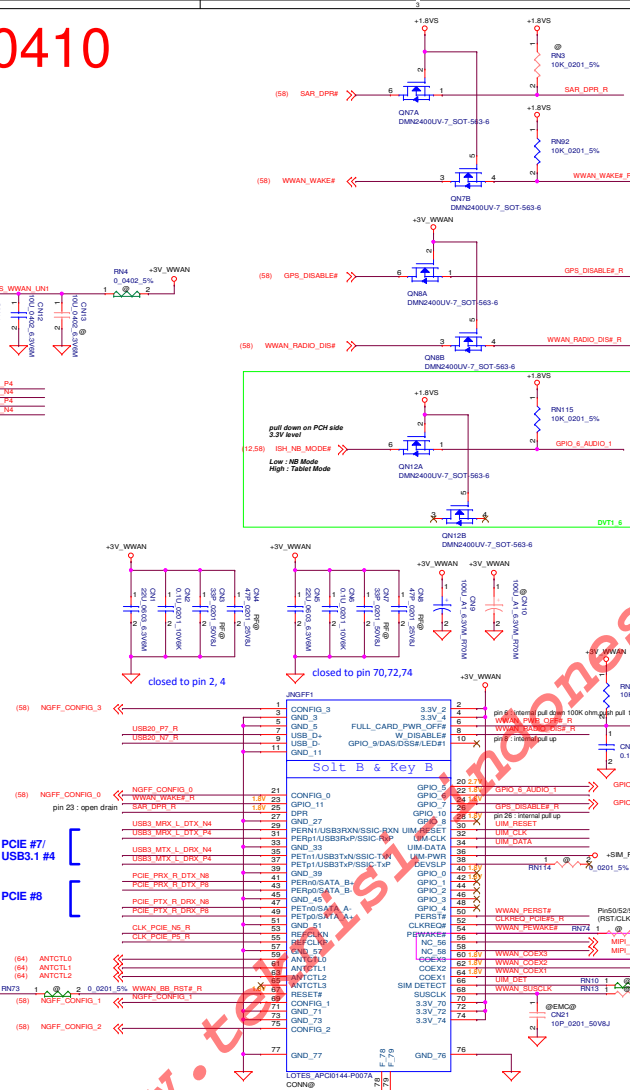
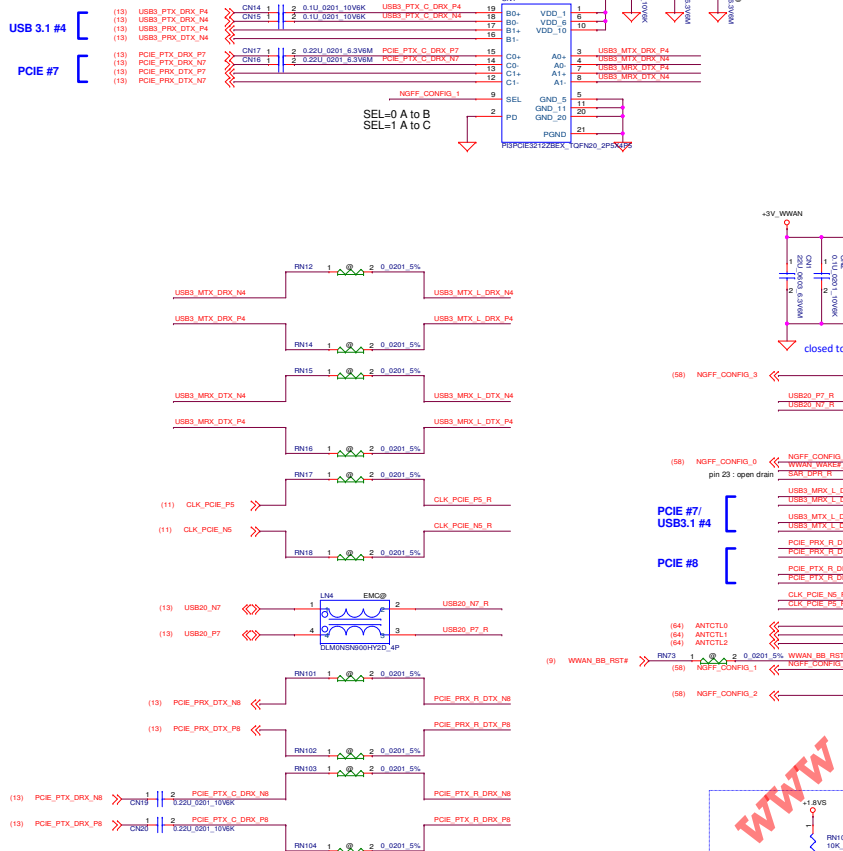
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				LA-G441P	



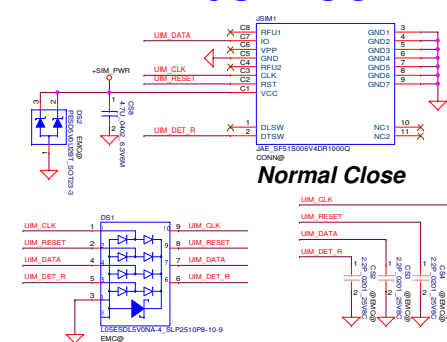
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## PCIe/USB 3.0 Mux

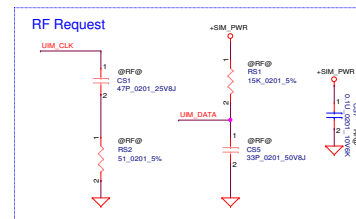
TABLE 2  
CIRCUIT DETECTION SWITCH AND DELAY SWITCH

	WITHOUT TRAY	TRAY MATED
DETECTION SWITCH		

## uSIM CONN



### **Normal Close**



RF Reques

State#	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	Port Configuration
	IP (21)	IP (29)	IP (75)	IP (1)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	HIGH	GND	GND	SSD - PCie	N/A
2	GND	GND	HIGH	GND	WWAN - PCie	0
3	GND	HIGH	HIGH	GND	WWAN - PCie	1
4	GND	GND	GND	HIGH	WWAN - USB 3.0	0
5	GND	HIGH	GND	HIGH	WWAN - USB 3.0	1
6	GND	GND	HIGH	HIGH	WWAN - USB 3.0	2
7	GND	HIGH	HIGH	HIGH	WWAN - USB 3.0	3
8	HIGH	GND	GND	GND	WWAN - SSIC	0
9	HIGH	HIGH	GND	GND	WWAN - SSIC	1
10	HIGH	GND	HIGH	GND	WWAN - SSIC	2
11	HIGH	HIGH	HIGH	GND	WWAN - SSIC	3
12	HIGH	GND	GND	HIGH	WWAN - PCie	0
13	HIGH	HIGH	GND	HIGH	WWAN - PCie	3
14	HIGH	GND	HIGH	HIGH	DDP/HCA - PCie	N/A
15	HIGH	HIGH	HIGH	HIGH	No Module	N/A

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			LIA-G441P 2/18/2018 63 of 100 6,100/00	

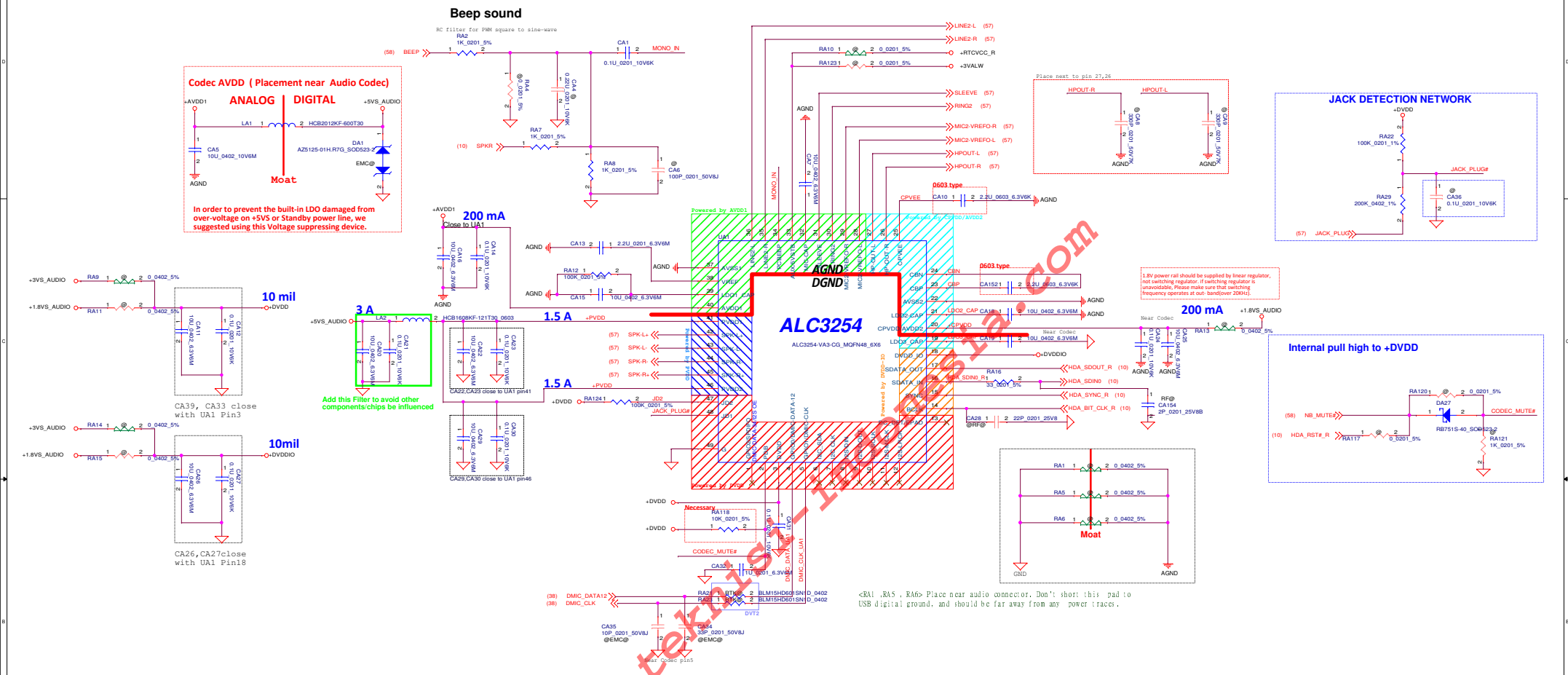
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				Rev	
				0.1(X00)	

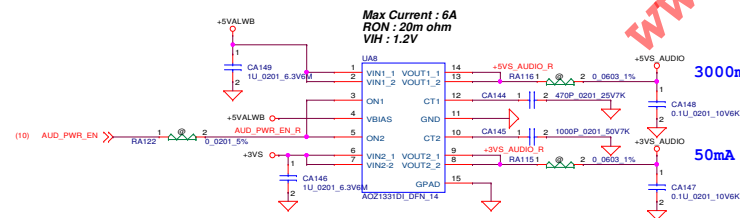
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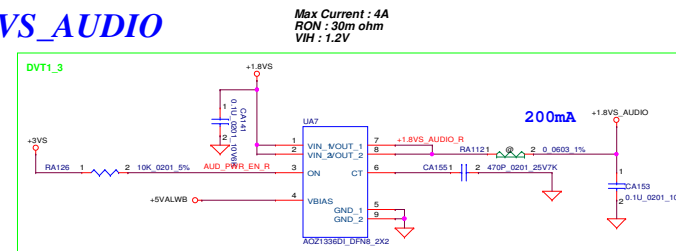


## 5VS\_AUDIO & 3VS\_AUDIO



C <sub>TX</sub> (pF)	Rise Time (μs) 10%~90%, C <sub>IN</sub> =0.1μF, C <sub>RNN</sub> =1μF, R <sub>ON</sub> =10Ω							
	Typical Values at 25°C, 25V X7R 10% Ceramic Cap.							
	V <sub>IN</sub> =5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V	
0	85	68	49	45	40	37	34	
220	431	297	172	147	122	106	89	
470	888	583	332	269	218	189	161	
1000	1700	1130	657	550	446	390	316	
2200	3805	2534	1347	1152	966	867	701	
4700	8053	5255	1987	2578	2101	1838	1483	
10000	18320	12350	5545	5545	4155	4155	3229	

## 1.8VS\_AUDIO

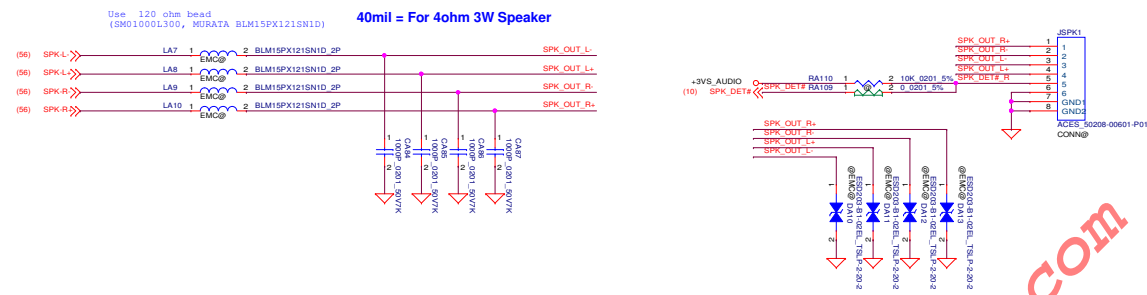


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			Size	Documents
			Rev	1.0000
			Date	LA-6441P
			Created	6/21/2018
			Issued	6/21/2018

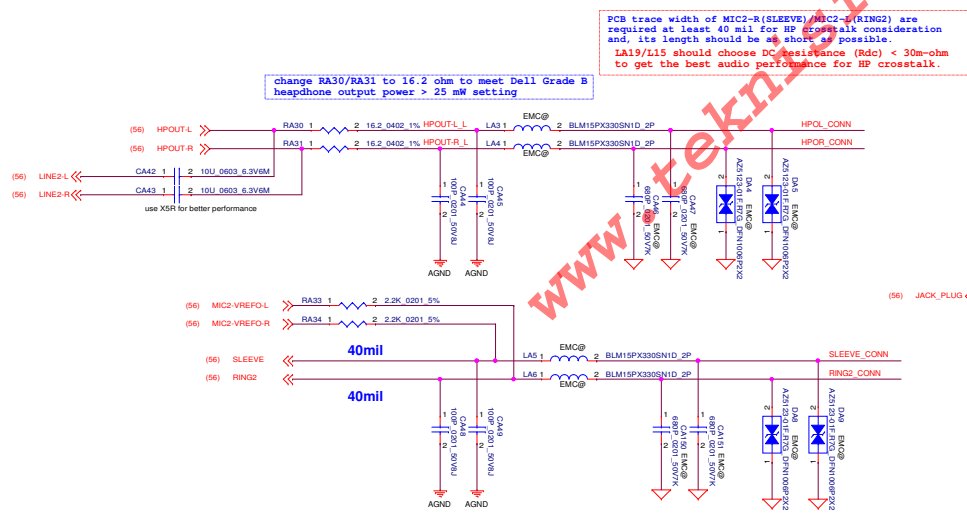


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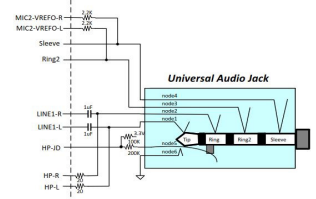
Int. Speaker Conn.



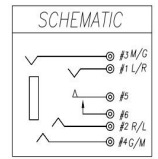
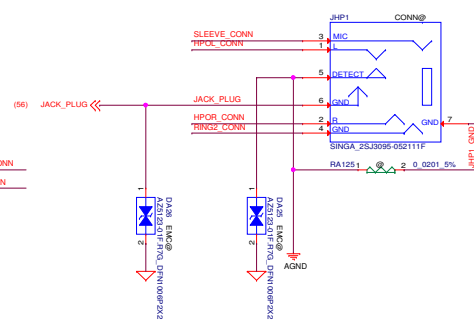
## Universal Audio Jack



## Analog Connector and Device

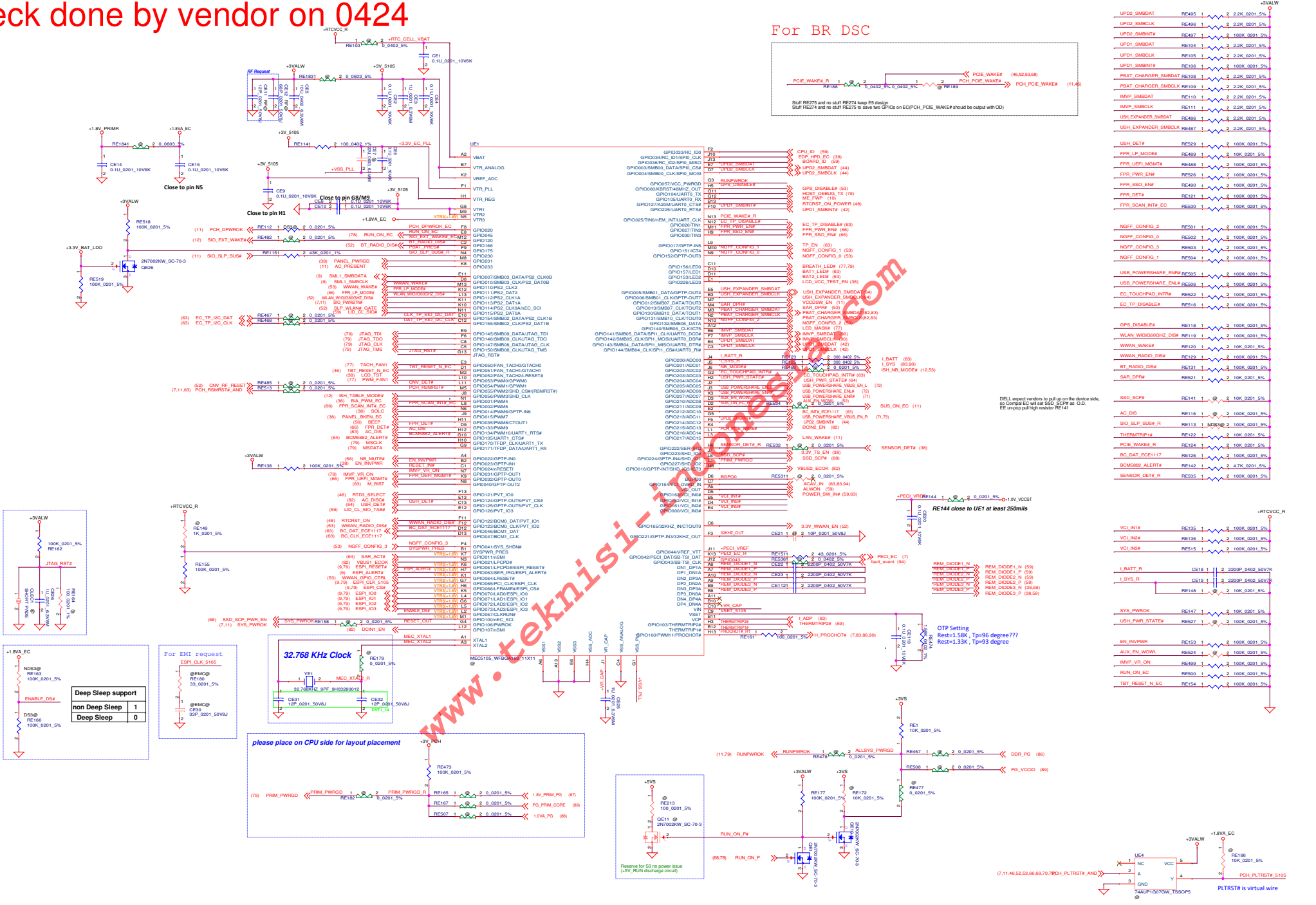


## Universal Audio Jack CONN



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For BR DSC





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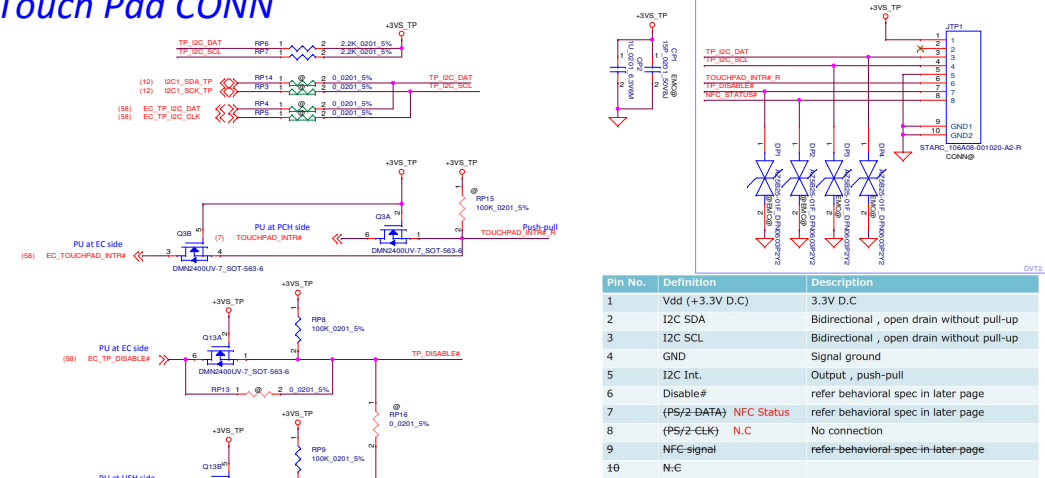
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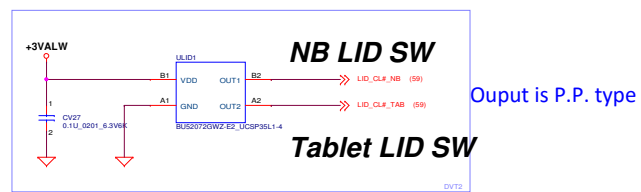
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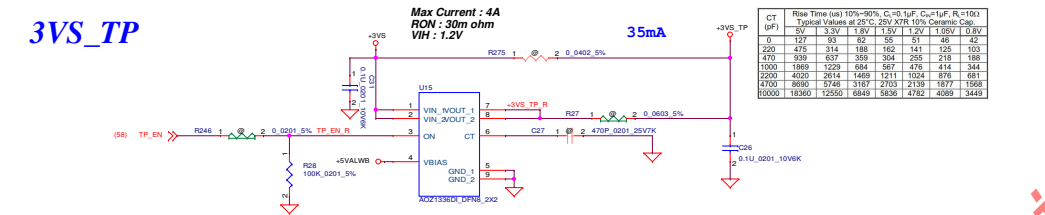
Touch Pad CONN



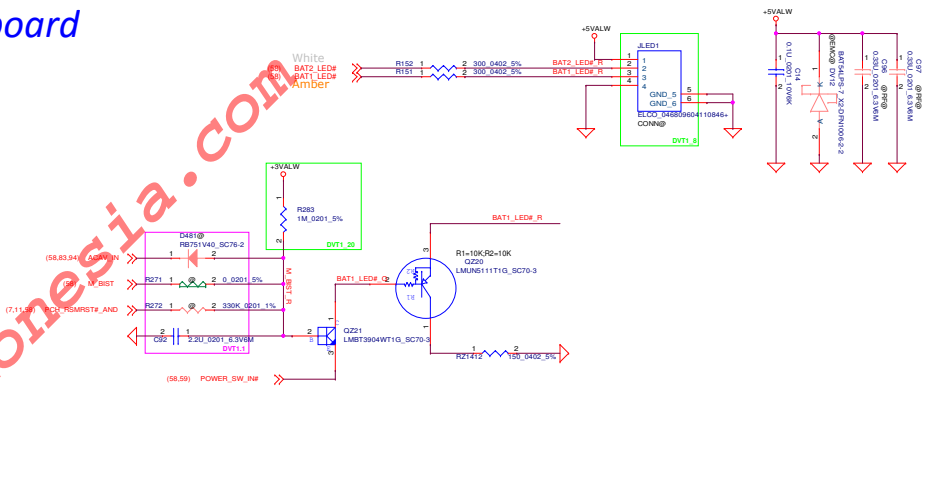
Hall Sensor (LID switch)



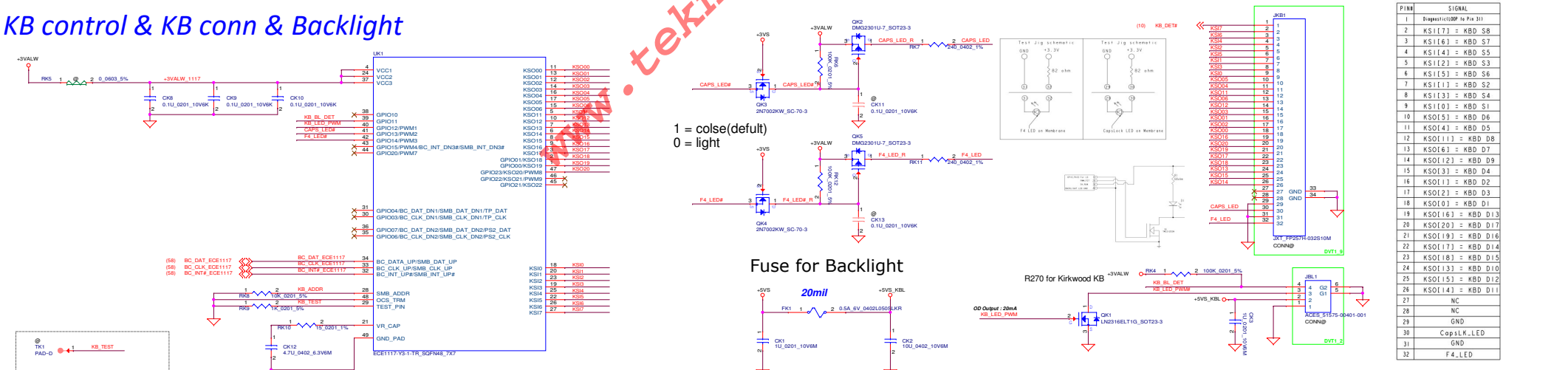
3VS\_TP



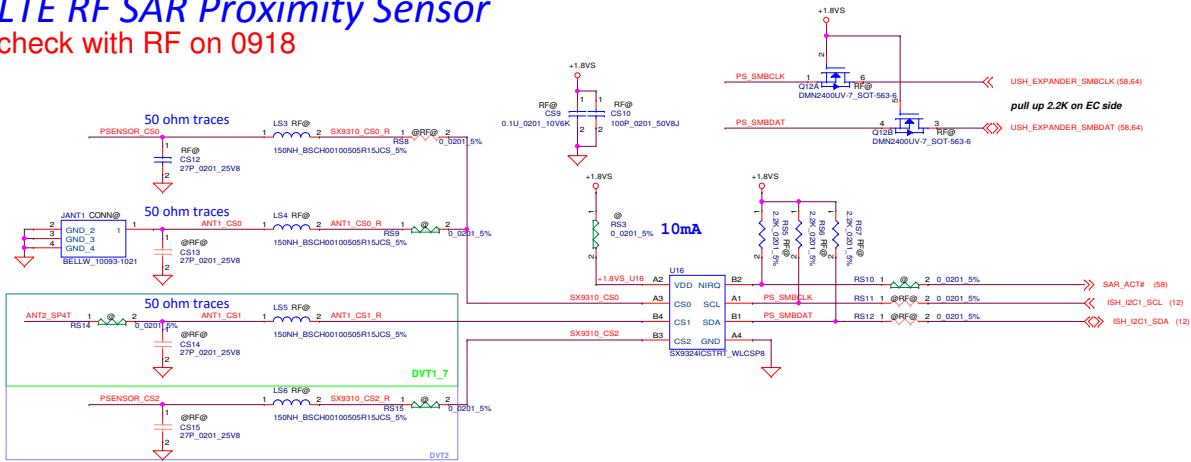
LED board



KB control & KB conn & Backlight



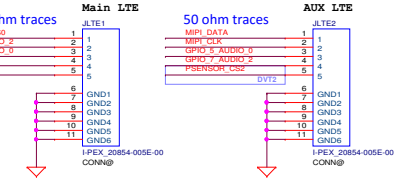
LTE RF SAR Proximity Sensor  
check with RF on 0918



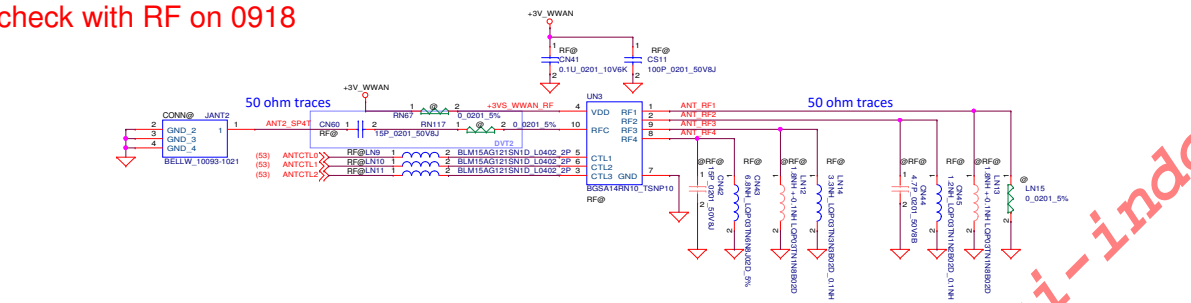
JLTE1/2 CONN



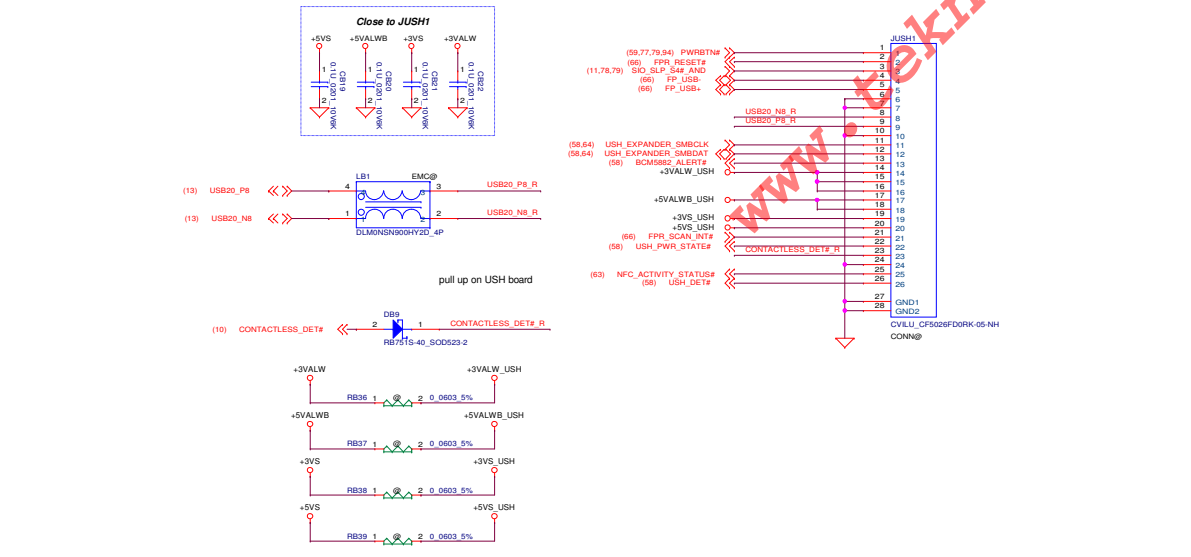
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LTE SW SP4T Tunnable IC  
check with RF on 0918



USH CONN





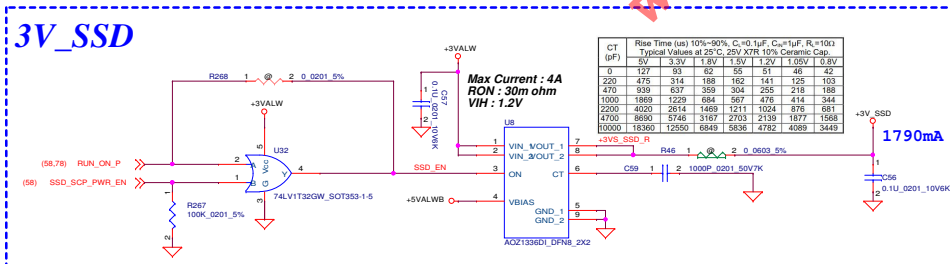
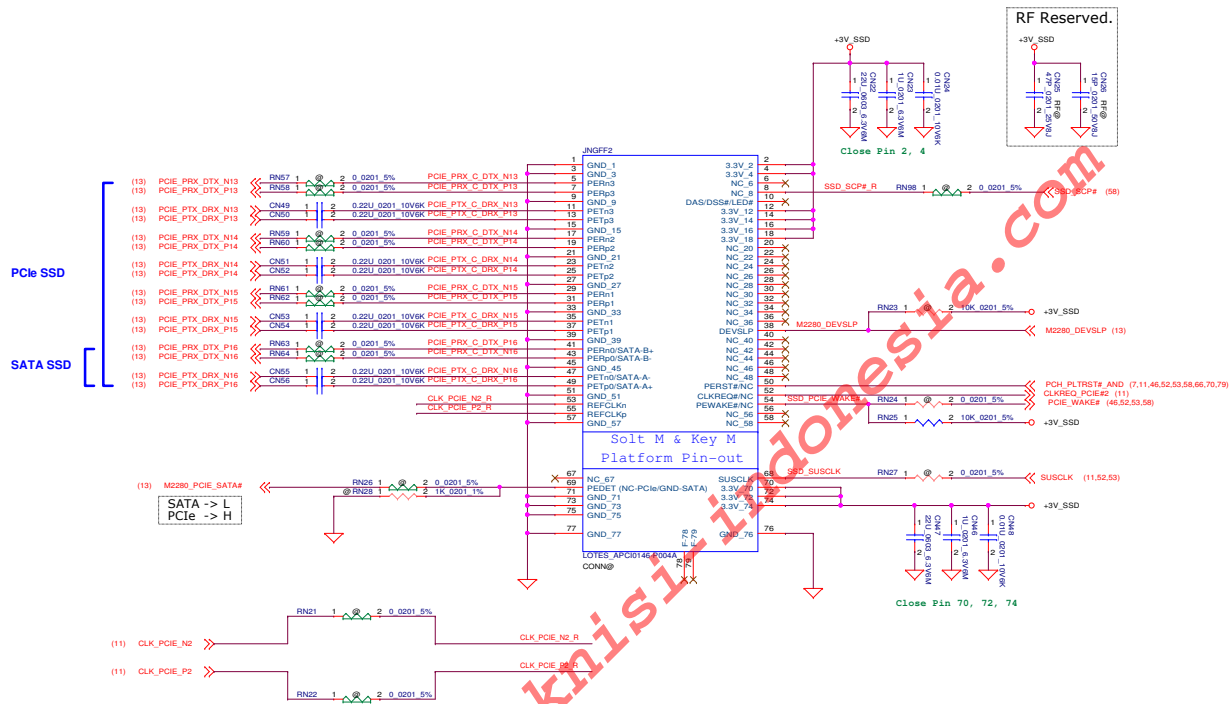
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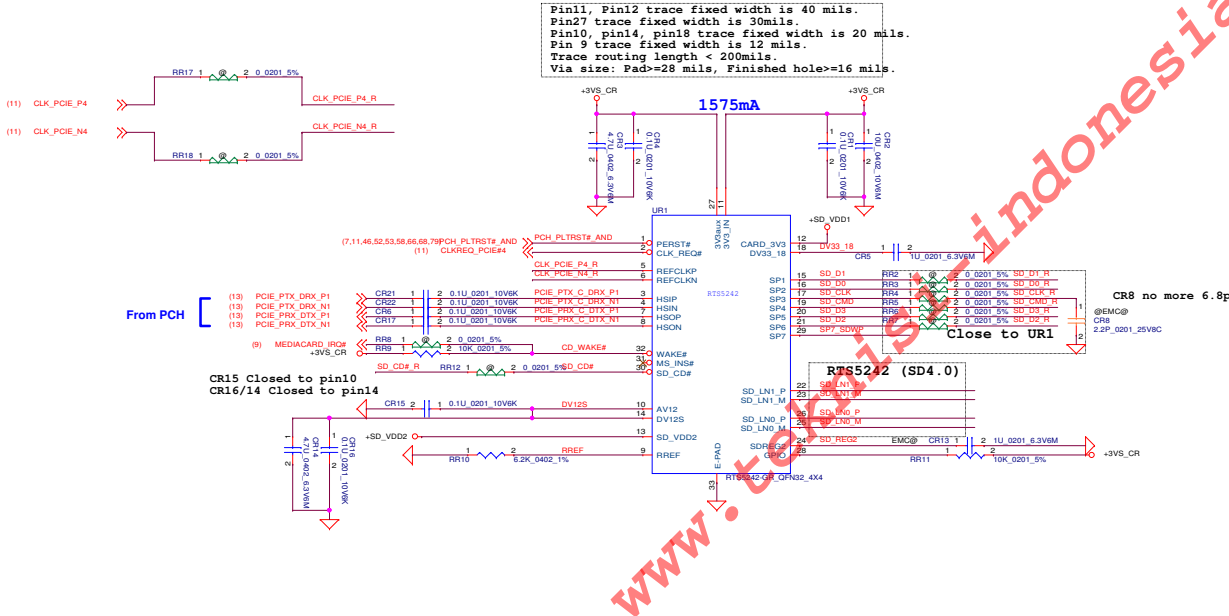
SN65 PCIe Redriver



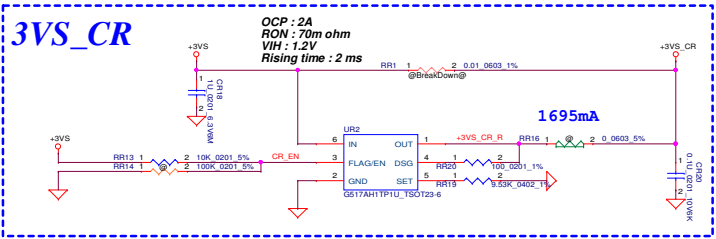
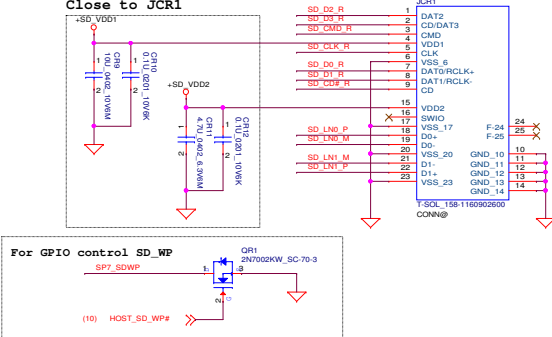
Check down by vendor on 0309

uSD Card Reader Controller/Connector

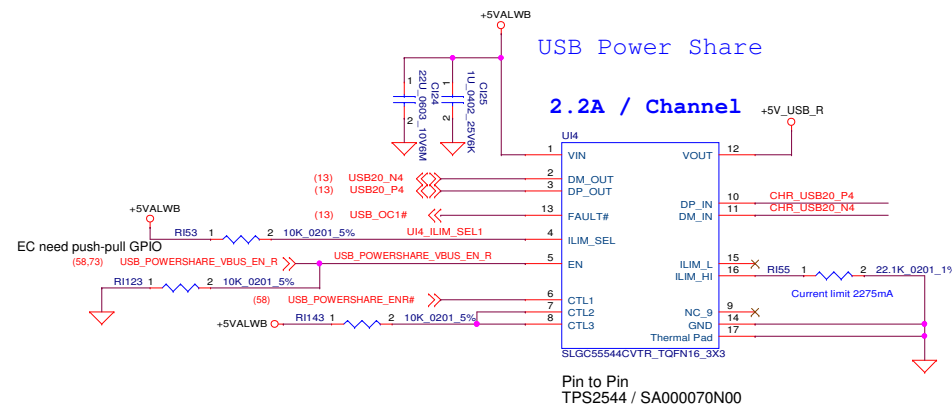
Contoller



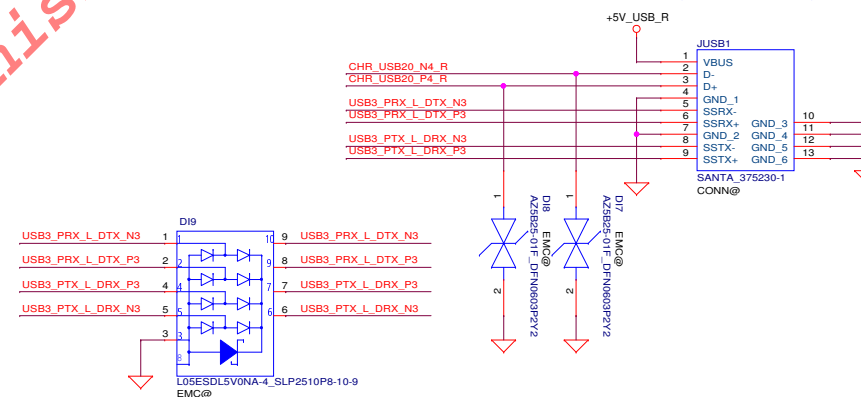
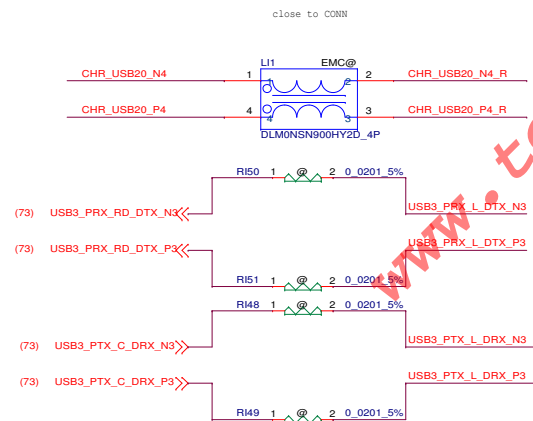
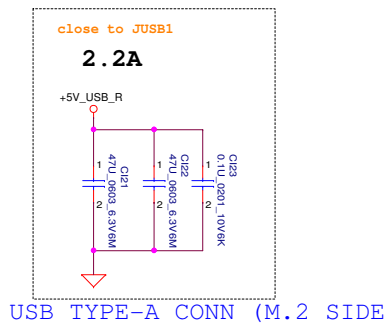
Connector



## USB Type-A Connector (M.2 SIDE)



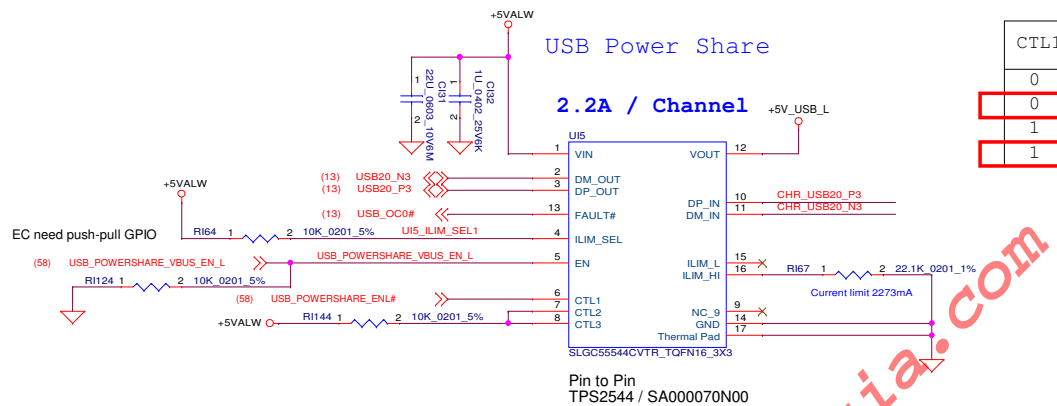
CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDP
1	1	1	1	CDP



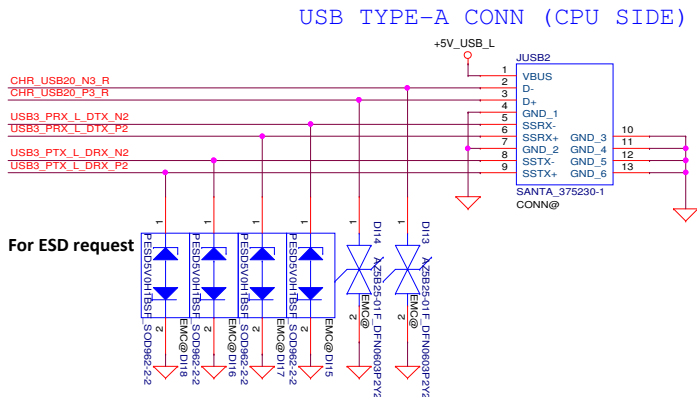
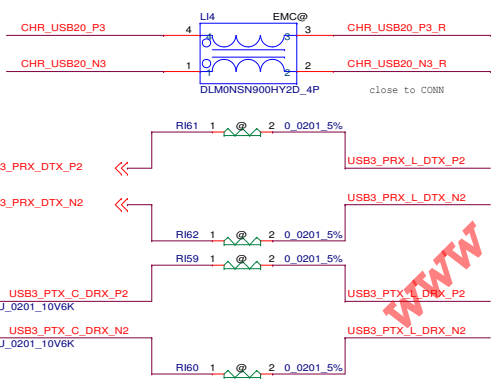
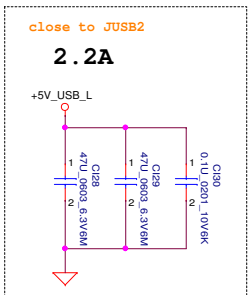
Security Classification		Compal Secret Data		<div style="text-align: right;"> <b>Compal Electronics, Inc.</b> </div>	
Issued Date	2015/12/16	Deciphered Date	2016/12/13	<div style="text-align: right;"> <b>P071 - USB3 TYPE-A PortA</b> </div>	
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				Document Number <b>LA-G41P</b>	
				Date: Friday, December 14, 2018      Sheet 71 of 100	

# Check done by vendor on 0321

## USB Type-A Connector (CPU Side)



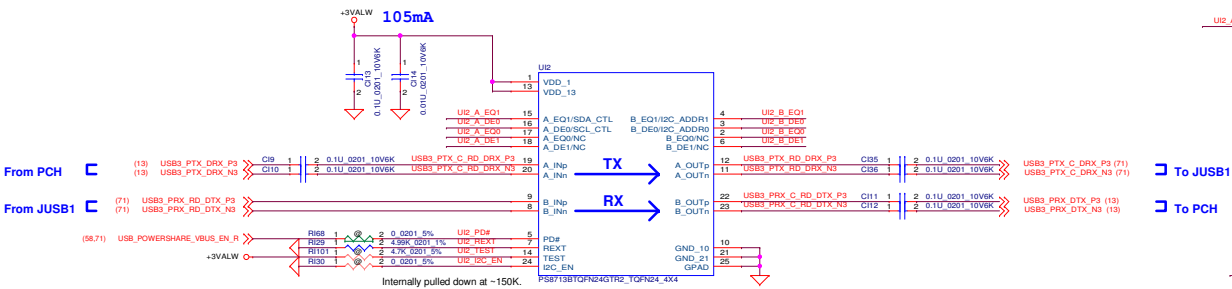
CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDP
1	1	1	1	CDP





Check done by vendor on 0309

USB3.0 Re-driver PS8713 (M.2 SIDE TO JUSB1)

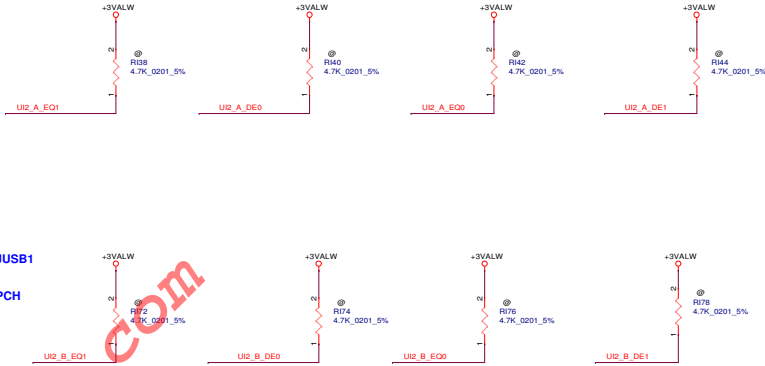


Parade\_PS8713B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ	A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	loss up to 9.5dB	0	0	0	0	3.5dB de-emphasis
0	1	0	1	loss up to 13dB	0	1	0	1	No de-emphasis
1	0	1	0	loss up to 4.5dB	1	0	1	0	2.7dB de-emphasis
1	1	1	1	loss up to 7.5dB	1	1	1	1	5dB de-emphasis

Both A\_EQ&B\_EQ have internal pull-down 150k

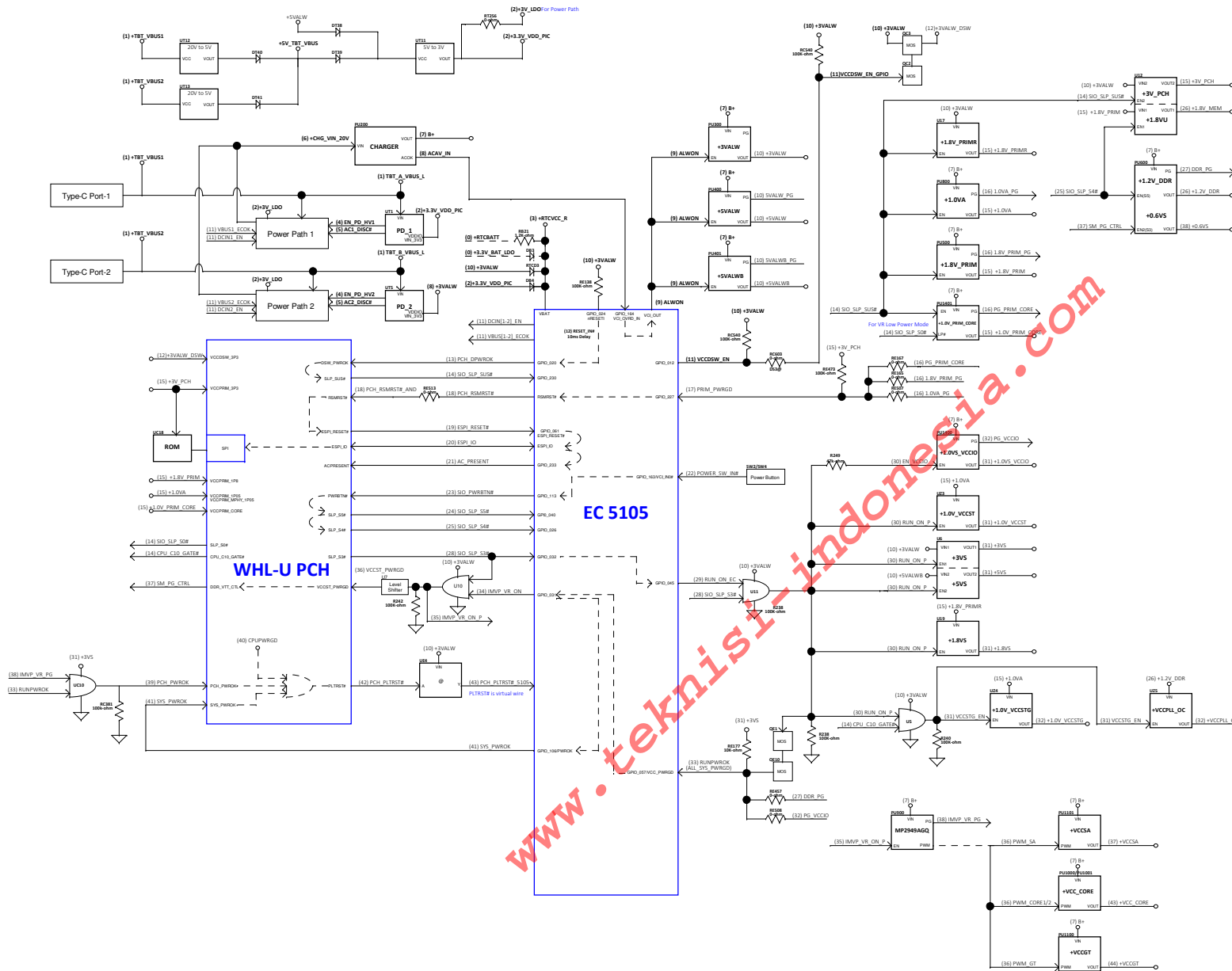
Both A\_DE&B\_DE have internal pull-down 150k

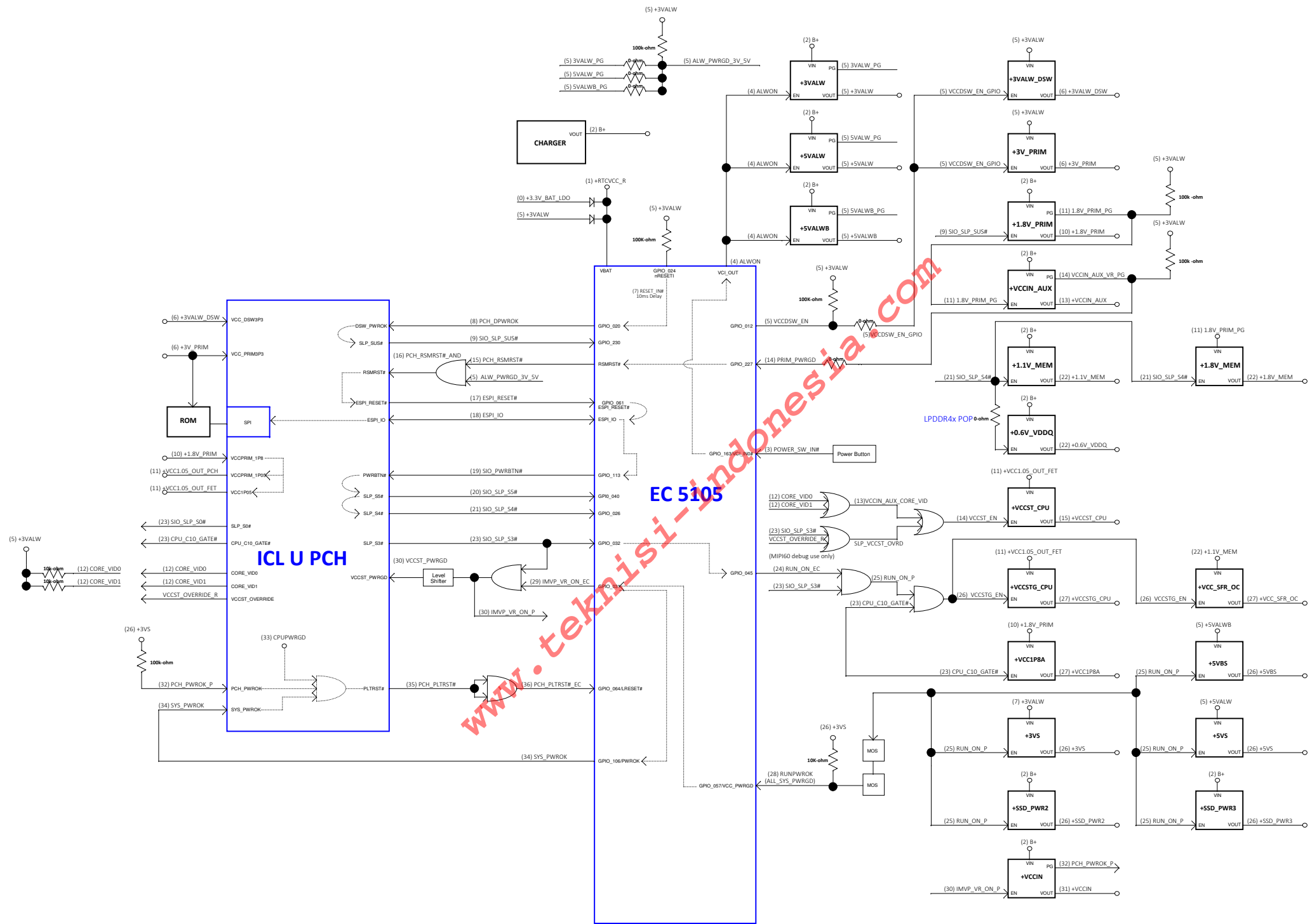


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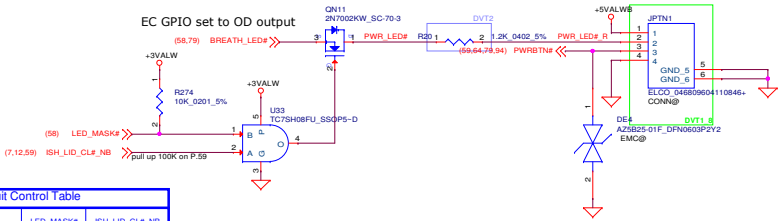
Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY	
Issued Date		Deciphered Date		Title	
2018/01/23		2022/12/31		P074 - Reserve	
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				Date	Rev
				Friday, December 14, 2018	0.1(X00)
				Sheet 74 of 100	





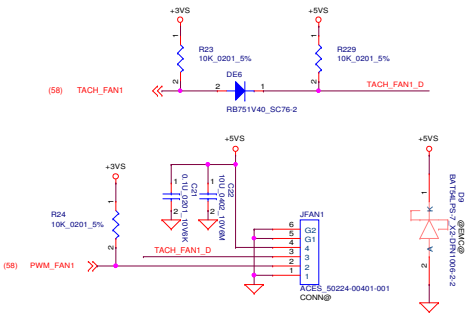
EC 5105

PW Switch Conn.

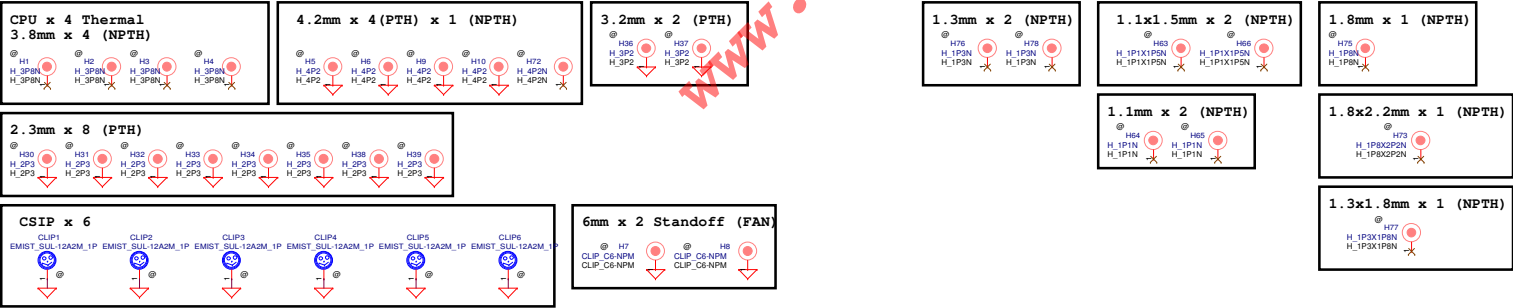


LED Circuit Control Table		
	LED_MASK#	6SH_LID_CLR_NB
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

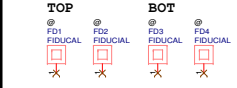
FAN1 ??need to check pin define



Screw Hole For ME 0507-2 update

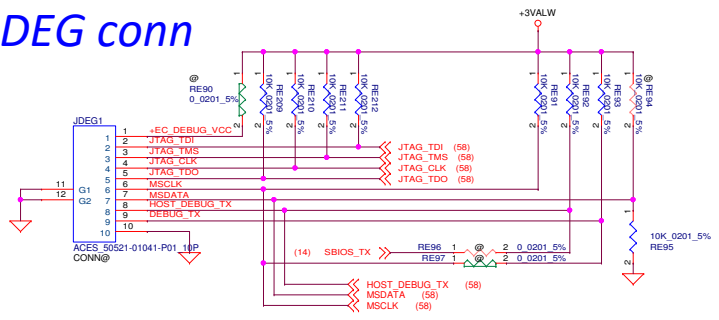


Fiducial Mark

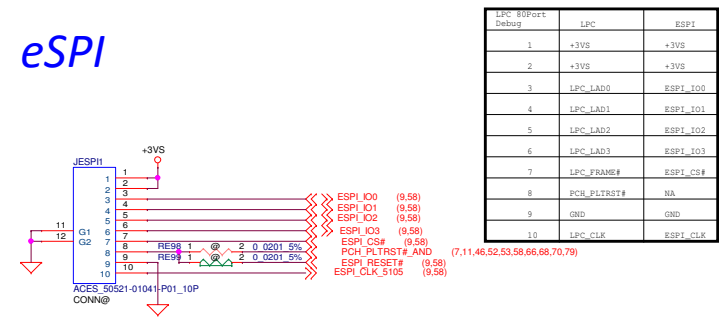




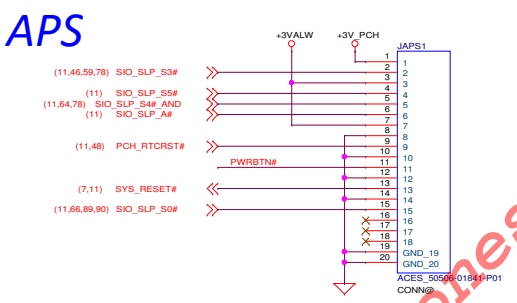
DEG conn



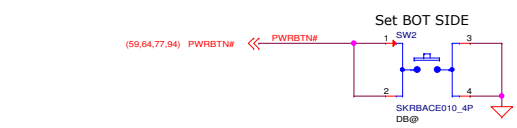
eSPI



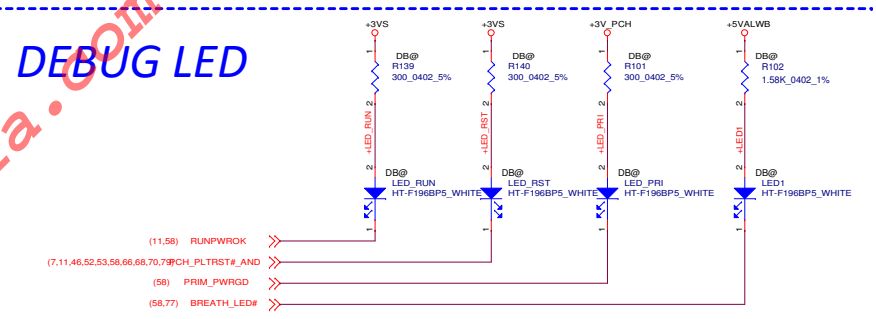
APS



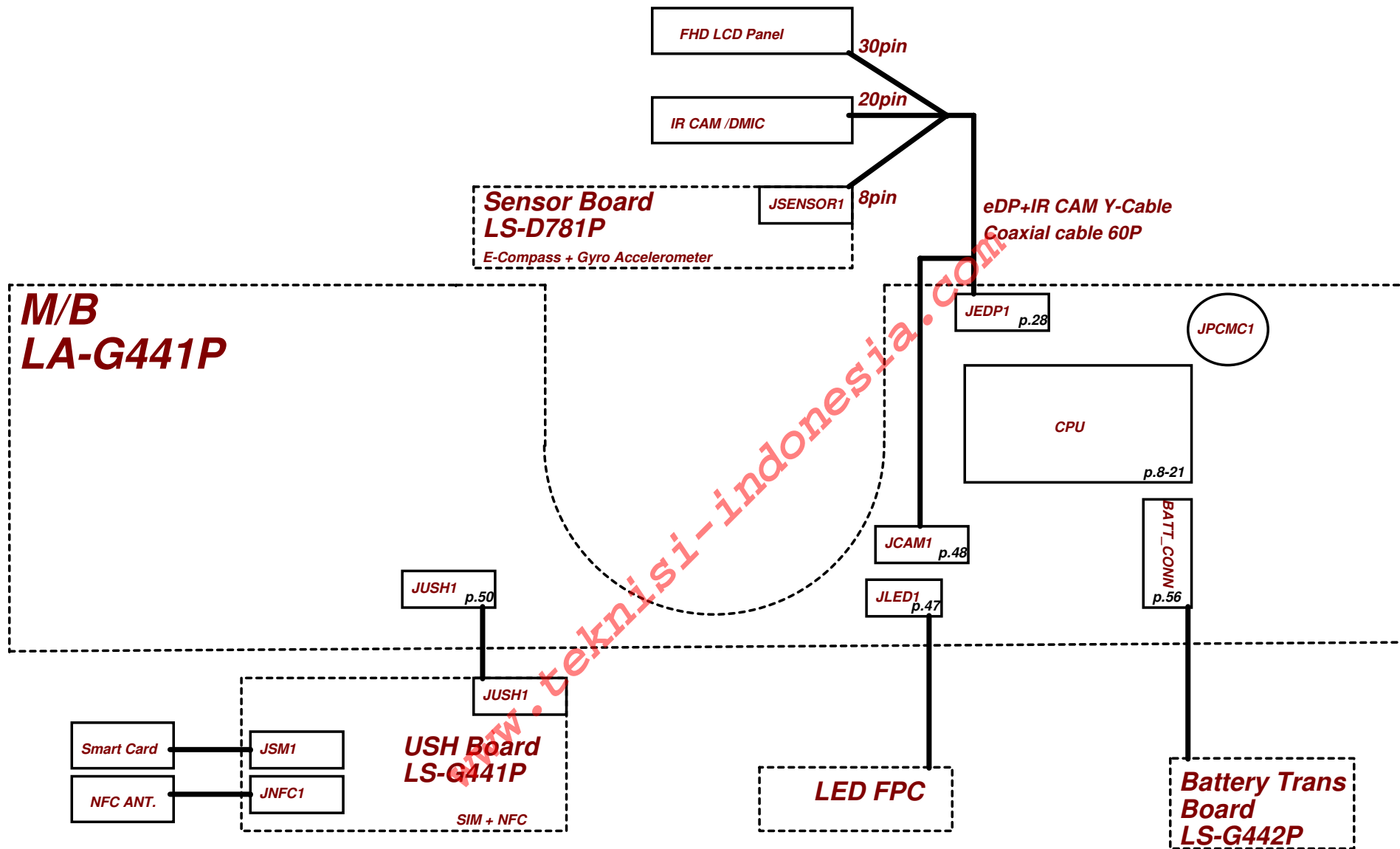
Test Power Button



DEBUG LED

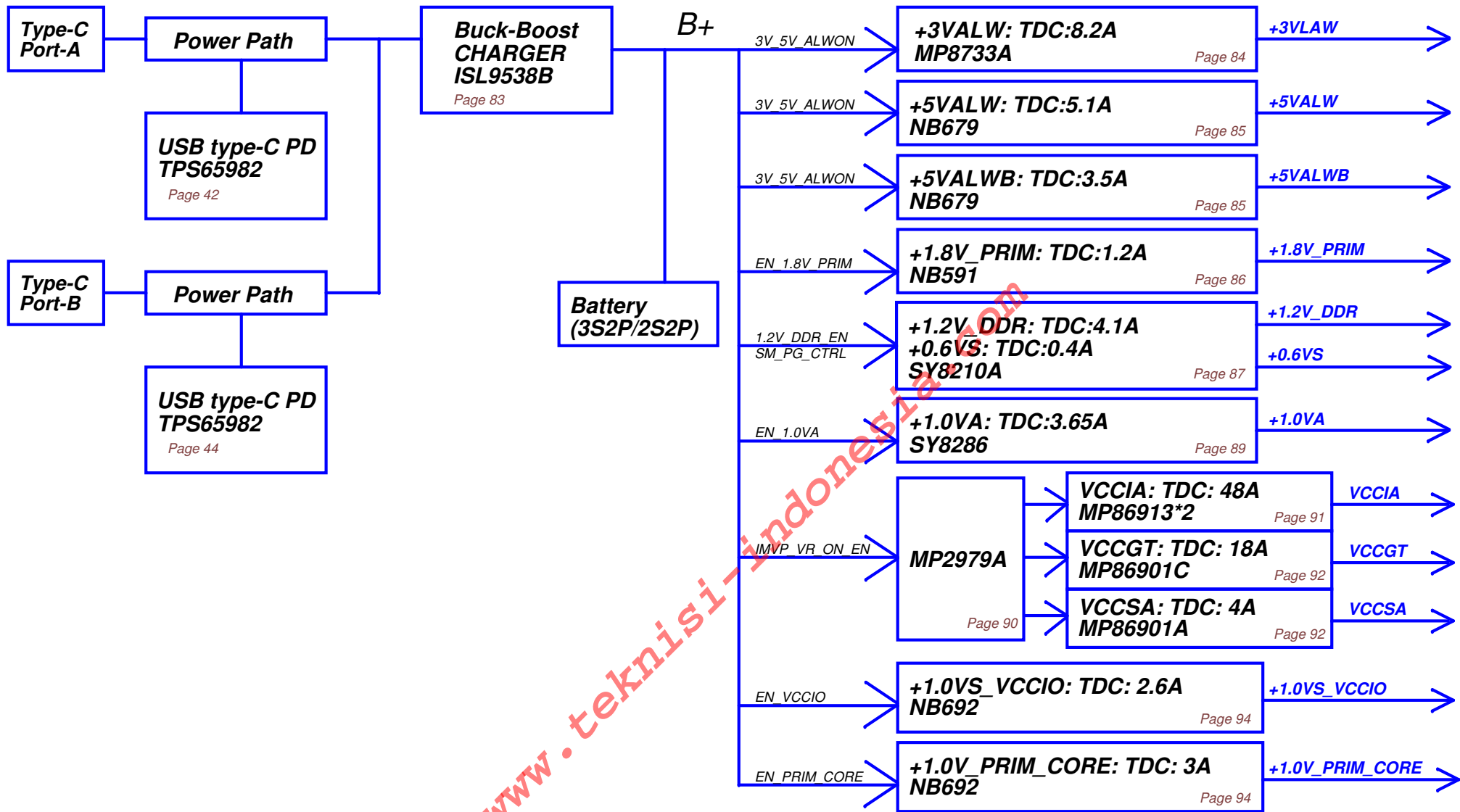


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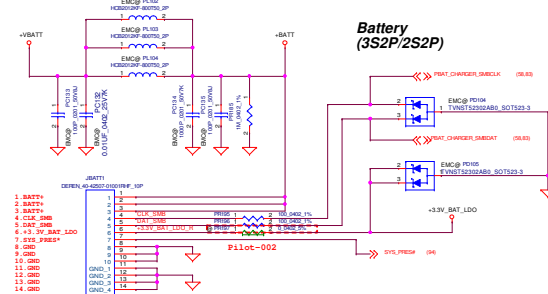
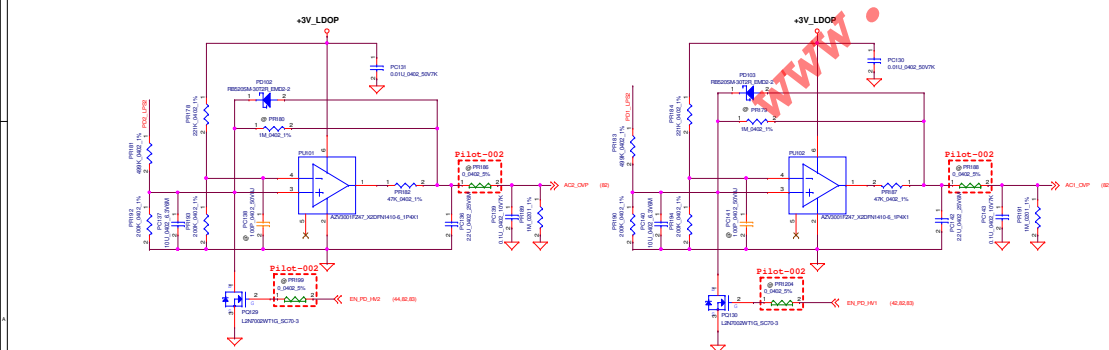
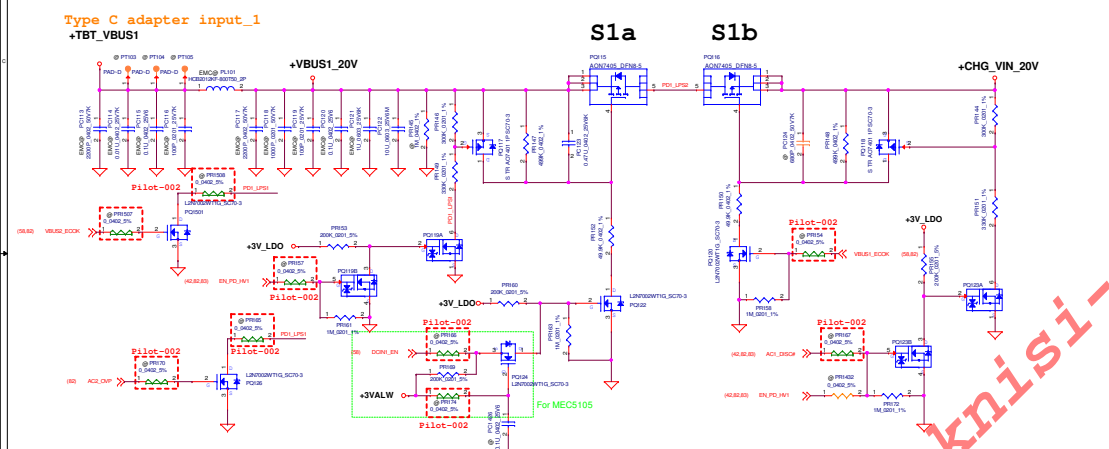
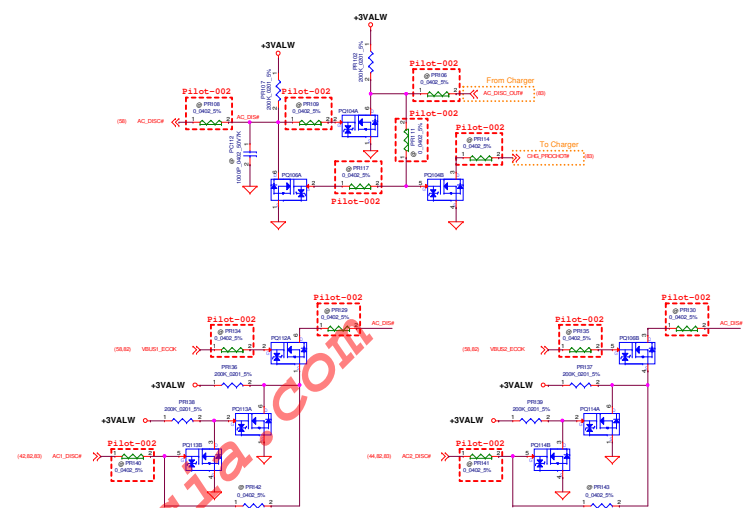
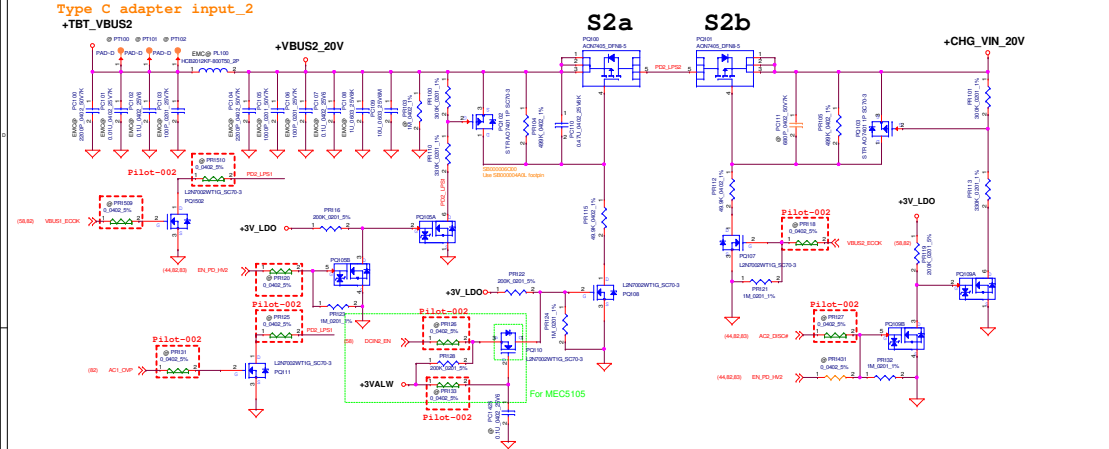


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		Date		Friday, December 14, 2018	
		Sheet		80 of 100	
				Rev	
				0.1(X00)	

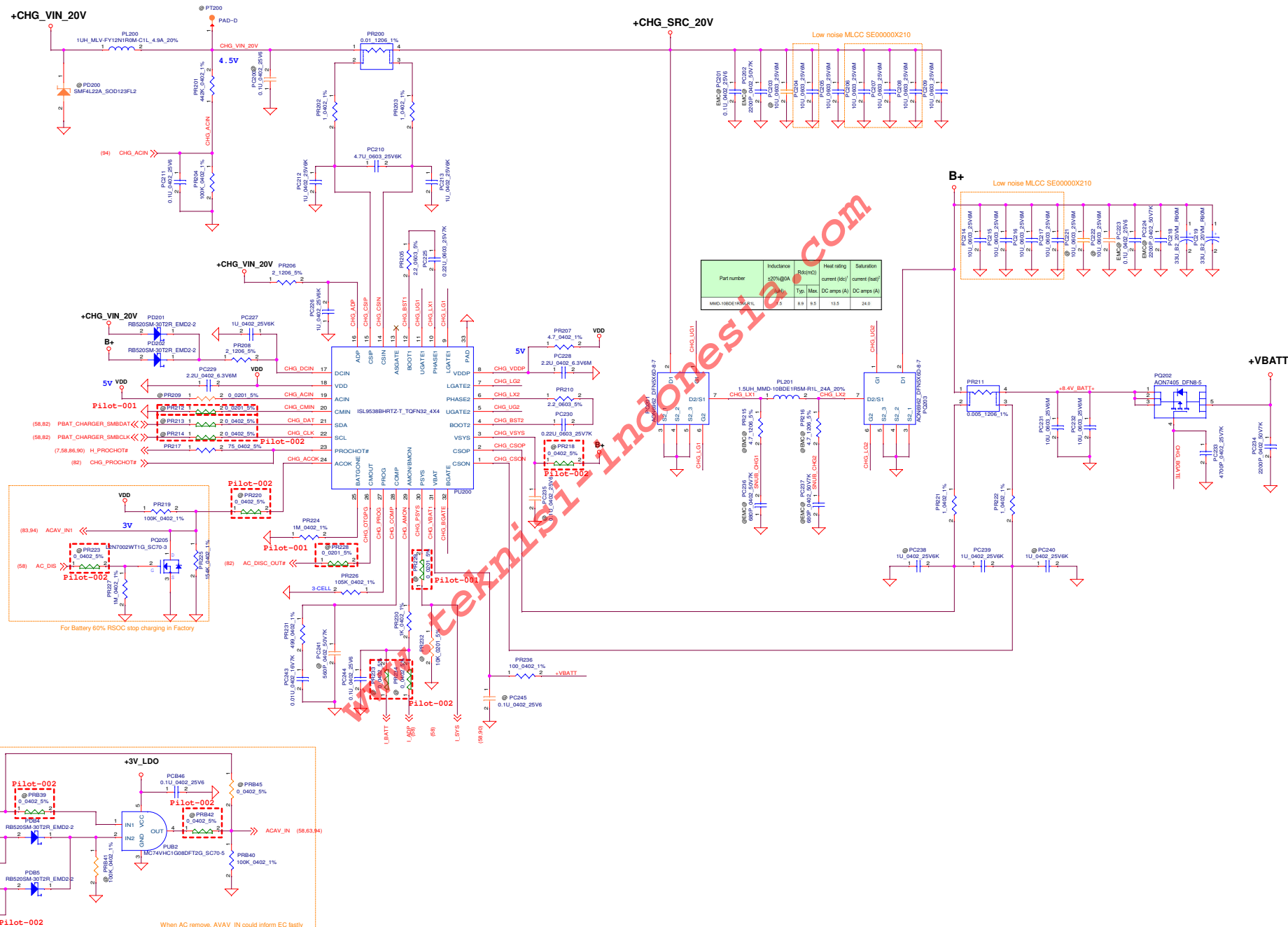




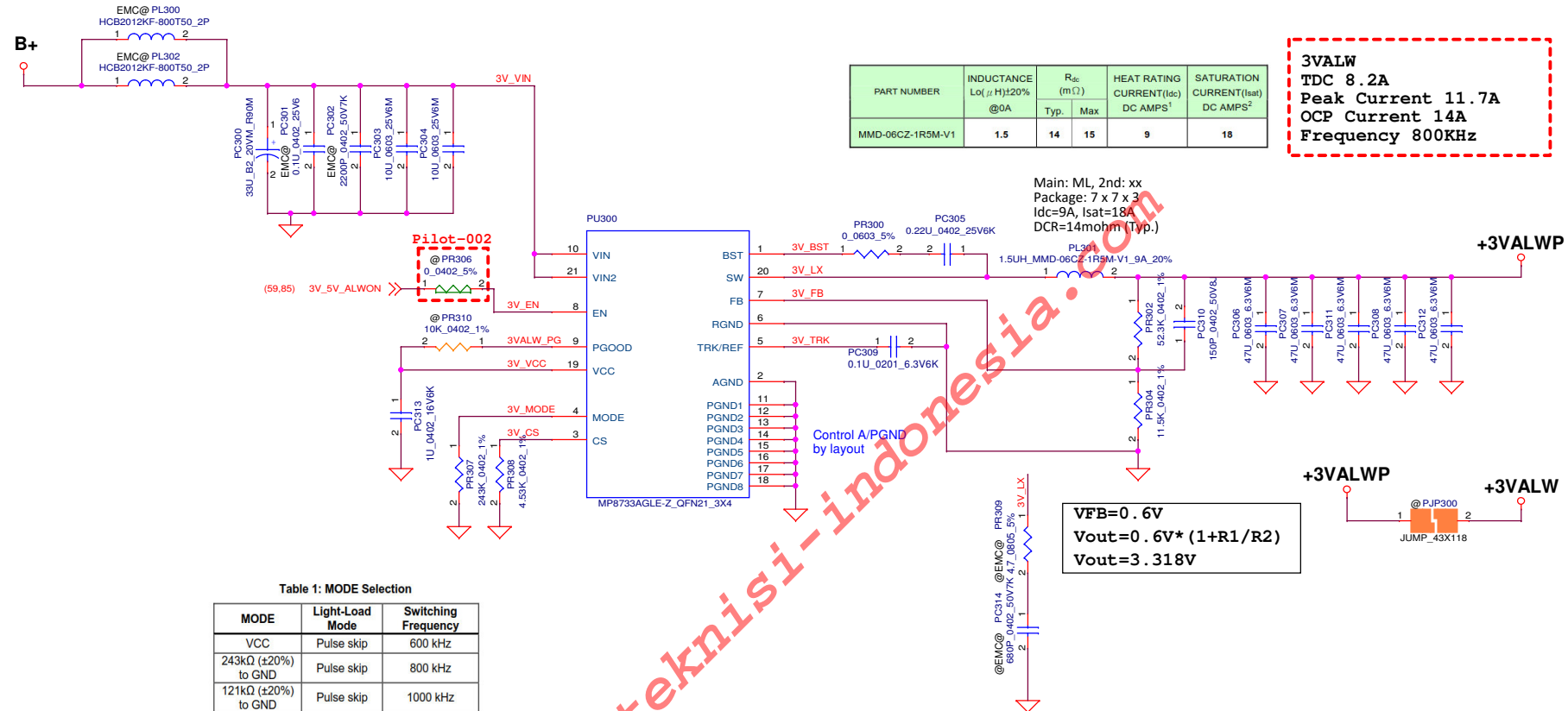
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Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title	P52-PWR Block Diagram
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				Date:	Friday, December 14, 2018
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				Rev	0.1



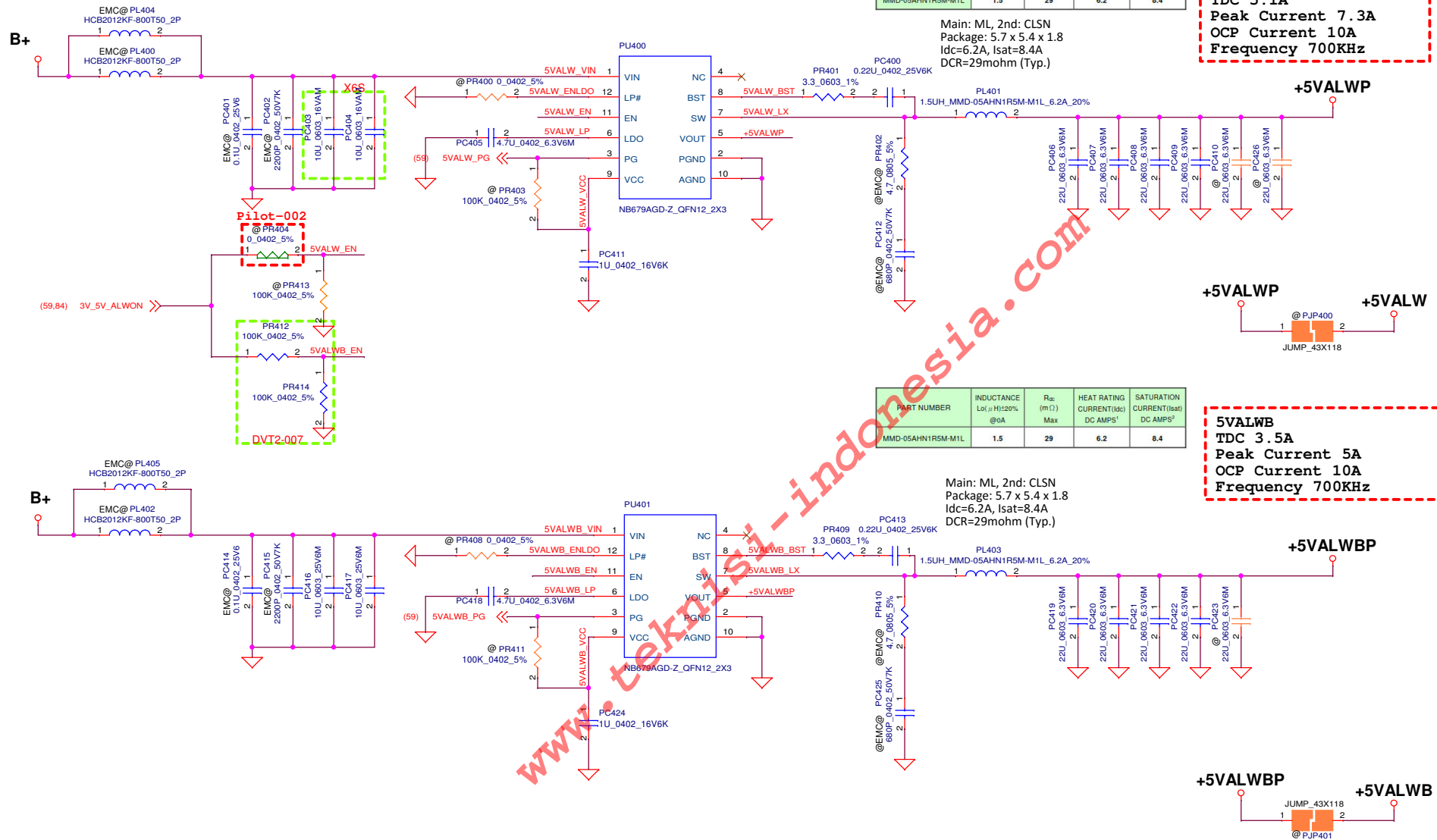
Security Classification	Compul Secret Data		Title	
Issued Date	2011/06/02	Deciphered Date	2013/01/28	Compul Electronics, Inc.
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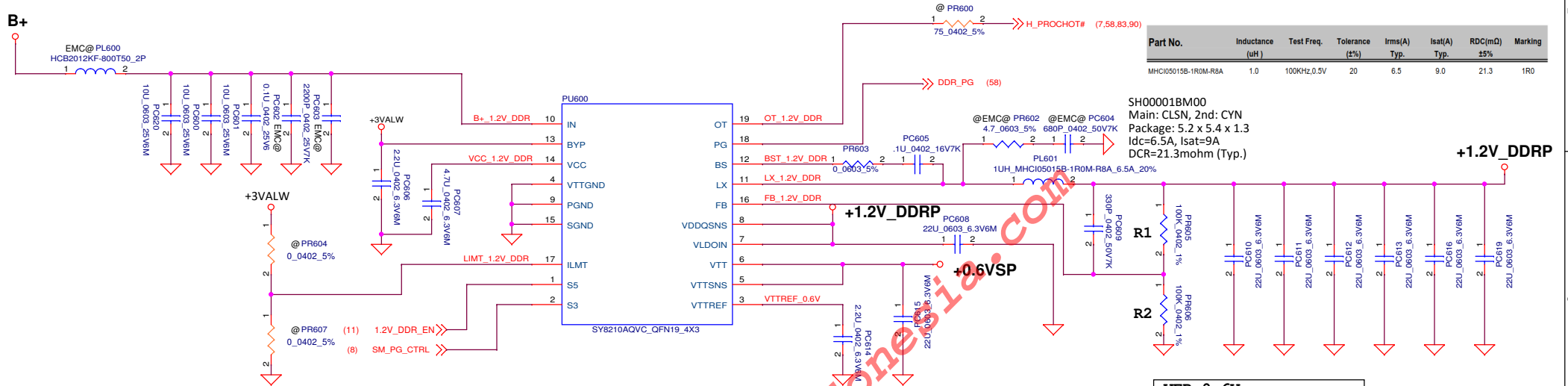
# 3V controller(35.1), Support component(35.2)



# 5V controller(35.1), Support component(35.2)



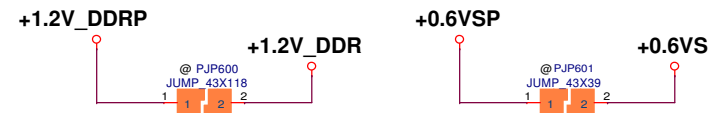
# DDR controller(35.3), Support component(35.4)



$$V_{FB}=0.6V$$

$$V_{out}=0.6V \cdot (1+R1/R2)$$

$$V_{out}=1.2V$$



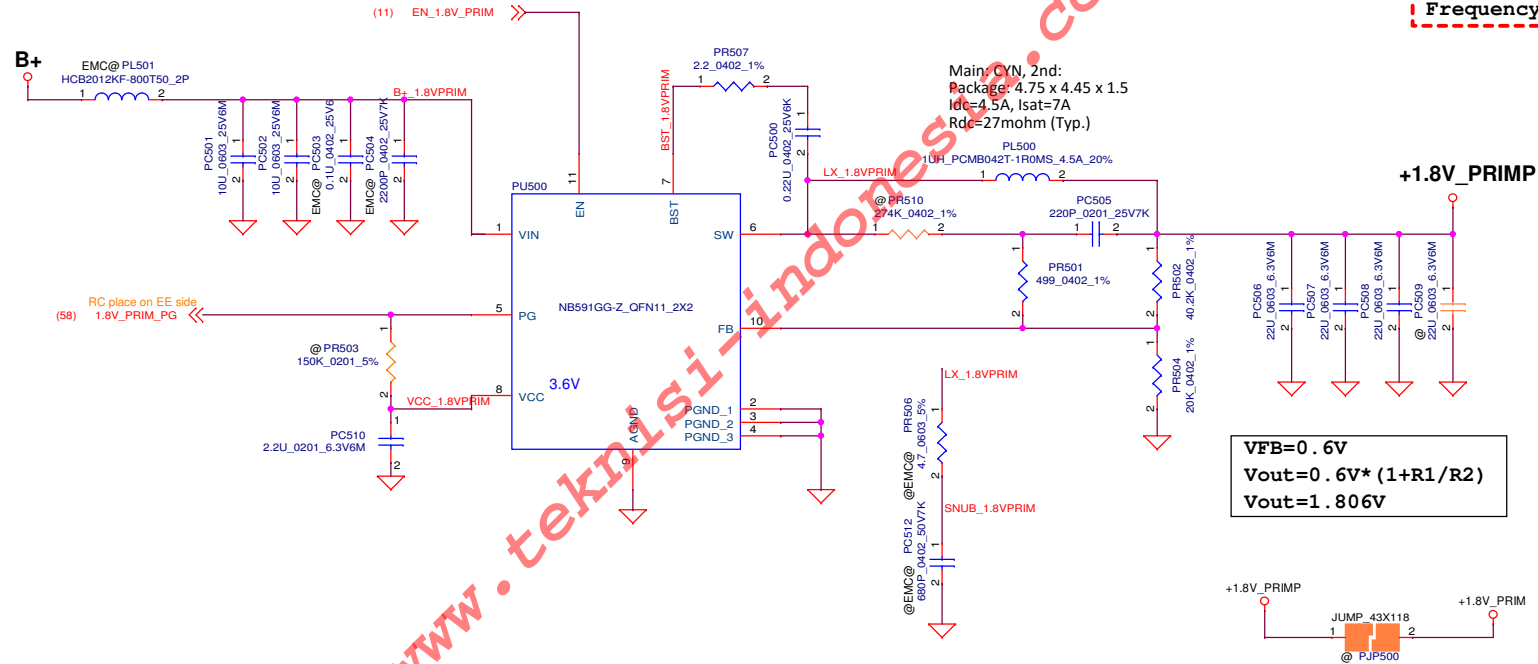
**+1.2V\_DDR**  
 TDC 4.1A  
 Peak Current 5.8A  
 OCP Current 12A  
 Frequency 600KHz

**+0.6VS**  
 TDC 0.4A  
 Peak Current 0.6A  
 OCP Current 2A (fix)  
 Frequency 600KHz

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Issued Date	2017/08/24	Deciphered Date	2017/08/24	Title	
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Size	Document Number	Rev		0.1	
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**+1.8V\_PRIM controller(35.13), Support component(35.14)**

1.8V\_PRIM  
TDC 1.2  
Peak Current 1.6A  
OCP 4A (Typ.)  
Frequency 750KHz

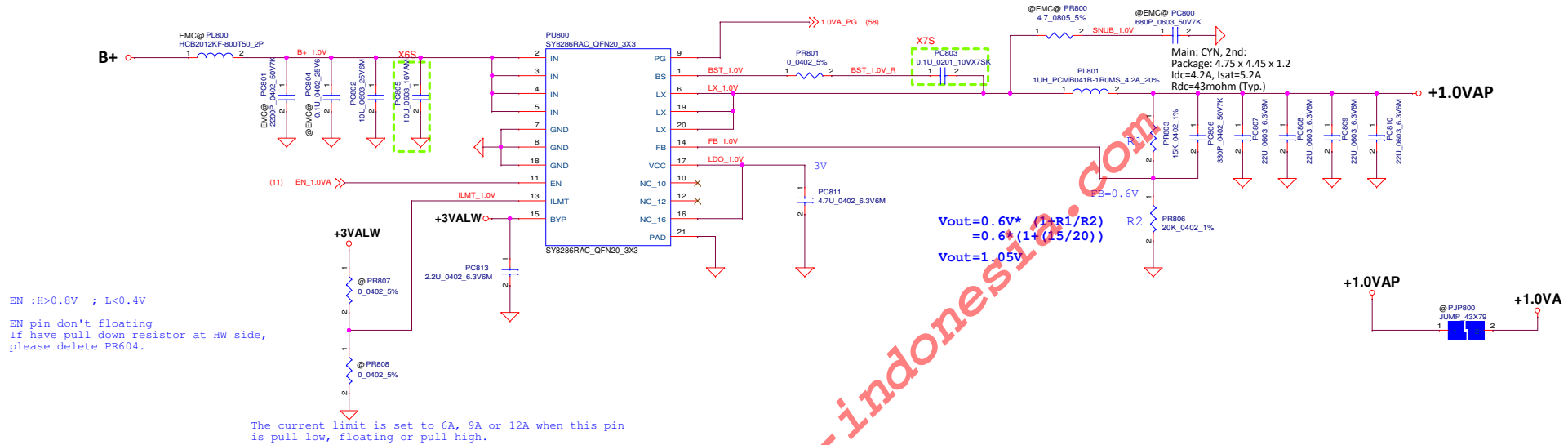


$$\begin{aligned} V_{FB} &= 0.6V \\ V_{out} &= 0.6V * (1 + R_1/R_2) \\ V_{out} &= 1.806V \end{aligned}$$

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>+1.8VPRIM</b>		
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1.05V controller(35.5), Support component(35.6)

```
+1.0VA
TDC 3.65A
Peak Current 5.2A
OCP current 9.0A
Frequency 500KHz
```



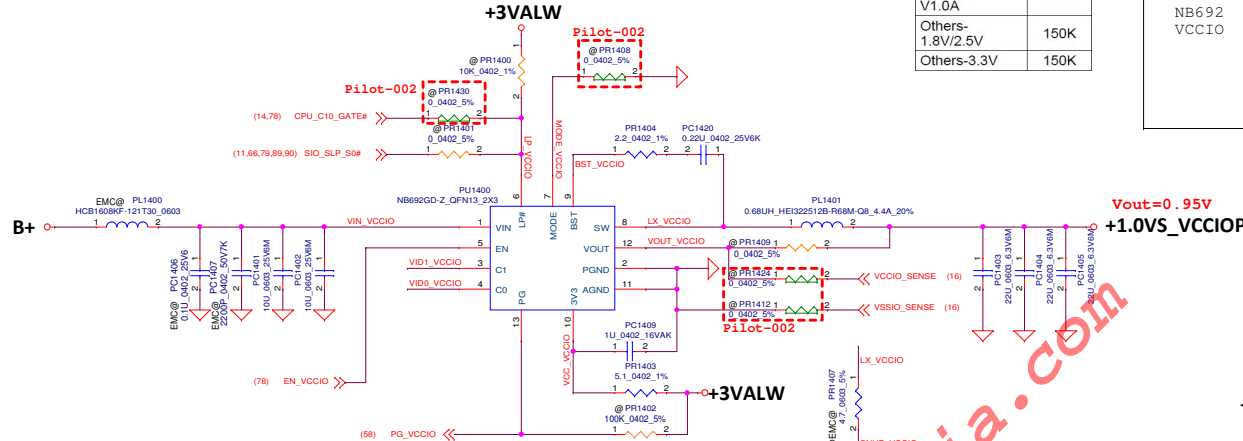
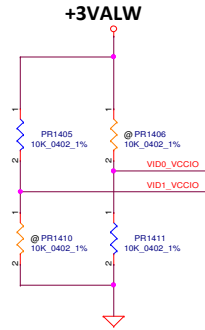
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title <b>+IVALW (SY8288)</b>		
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				<b>LA-E671P</b>		
Date:	Friday, December 14, 2018			Sheet	88	of 100



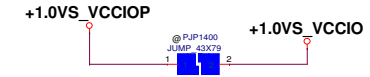
VCCIO controller(35.37), Support component(35.38)

V <sub>OUT</sub> (V)	R <sub>Mode</sub> (Ω)
VCCIO	0
PRIMCORE	Float
EDRAM/ EOPIO/ V1.0A	100K
Others- 1.8V/2.5V	150K
Others-3.3V	150K

	LPM	VID1	VID0	Vout
NB692 VCCIO	0	X	X	0 (LPM)
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975



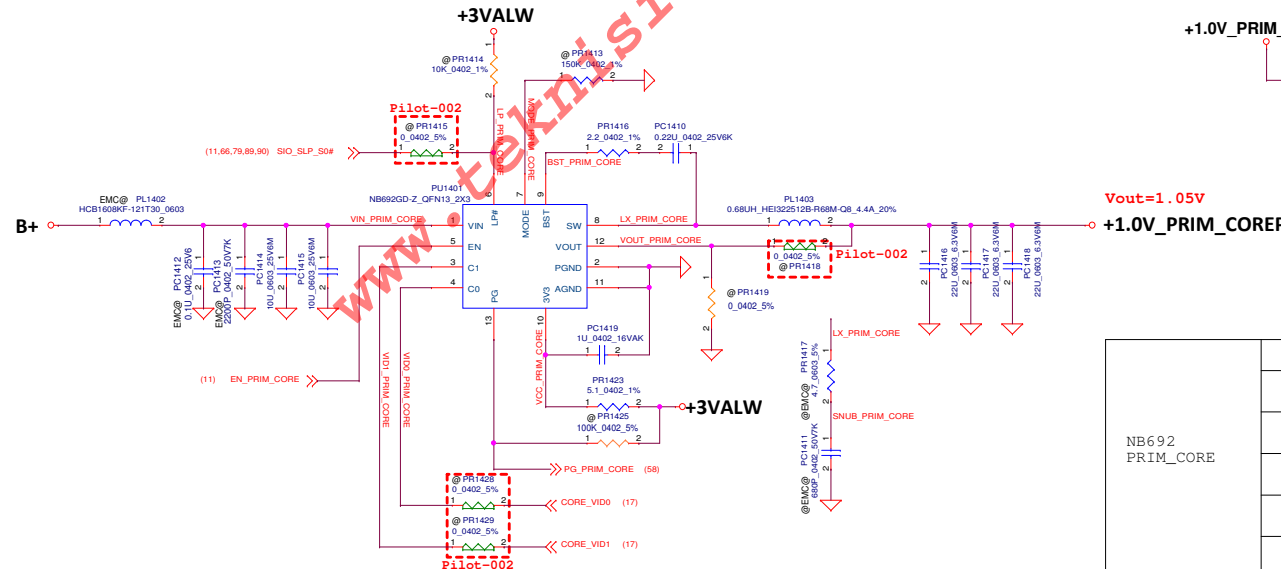
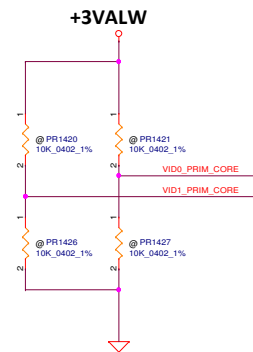
VCCIO  
TDC 2.6A  
Peak Current 3.7 A  
OCP Current 7.6 A Fix by IC  
MIN:7A  
MAX:8.5A  
Frequency:750KHz



PRIM\_CORE  
TDC 3A  
Peak Current 4.3 A  
OCP Current 7.6 A Fix by IC  
MIN:7A  
MAX:8.5A  
Frequency:750KHz



+1.0V\_PROM controller(35.35), Support component(35.36)



Vout=1.05V  
+1.0V\_PRIM\_COREP

	LPM	VID1	VID0	Vout
NB692 PRIM_CORE	0	X	X	0.75 (LPM)
	1	0	0	0.9
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05

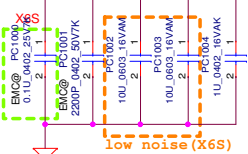
+1.0VS\_VCCIO controller(35.21), Support component(35.22)  
+1.0V\_PRIM\_CORE controller(35.23), Support component(35.24)

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1	1	1		89	1.0
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VCC\_CORE Dr. MOS (36.2), Support component(36.3)

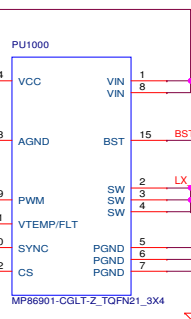
IA1\_B+



+3VALW

Pilot-002

(90) PWM\_CORE1  
(90,91,92) VRACPU\_VTEMP  
(90,91,92) SYNC  
(90) CS\_CORE1

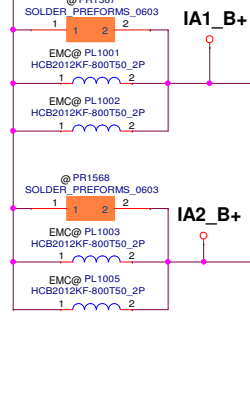


VCCIA (Base on PDG rev 0.9)  
Peak Current 70A (ICCmax)  
PL2 TDC :48A  
DC Load line :1.8mV/A  
AC Load line :1.8mV/A  
OCP Current 84A  
Fsw=1.5MHz

Main: CLSN, 2nd:  
Package: 7.5 x 6.9 x 2.4  
Idc=27A, Isat=42A  
Rdc=0.88mohm +/-5%

+VCC\_CORE

B+



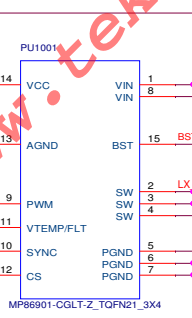
IA2\_B+

IA2\_B+

+3VALW

Pilot-002

(90) PWM\_CORE2  
(90,91,92) VRACPU\_VTEMP  
(90,91,92) SYNC  
(90) CS\_CORE2

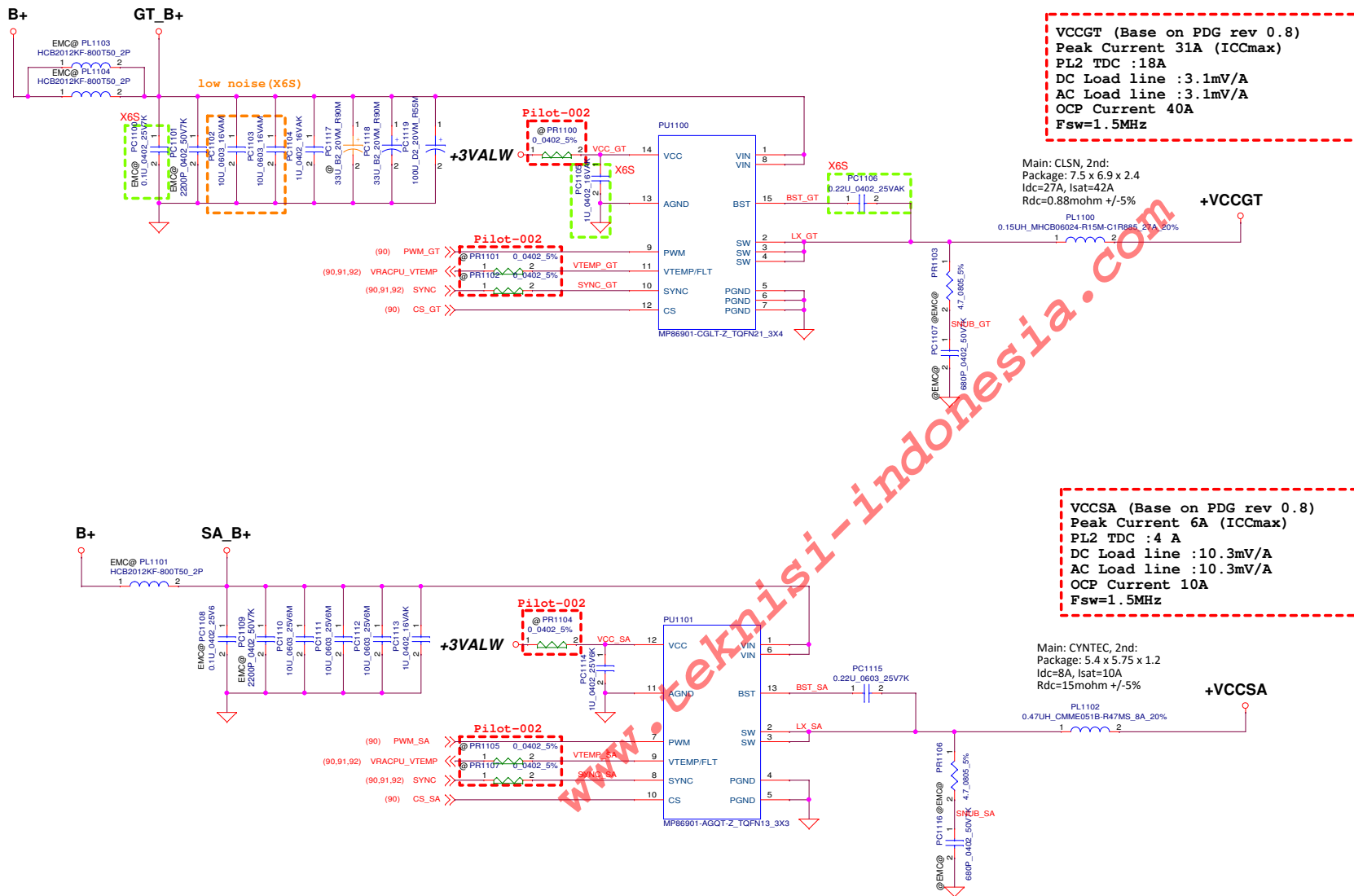


Main: CLSN, 2nd:  
Package: 7.5 x 6.9 x 2.4  
Idc=27A, Isat=42A  
Rdc=0.88mohm +/-5%

+VCC\_CORE

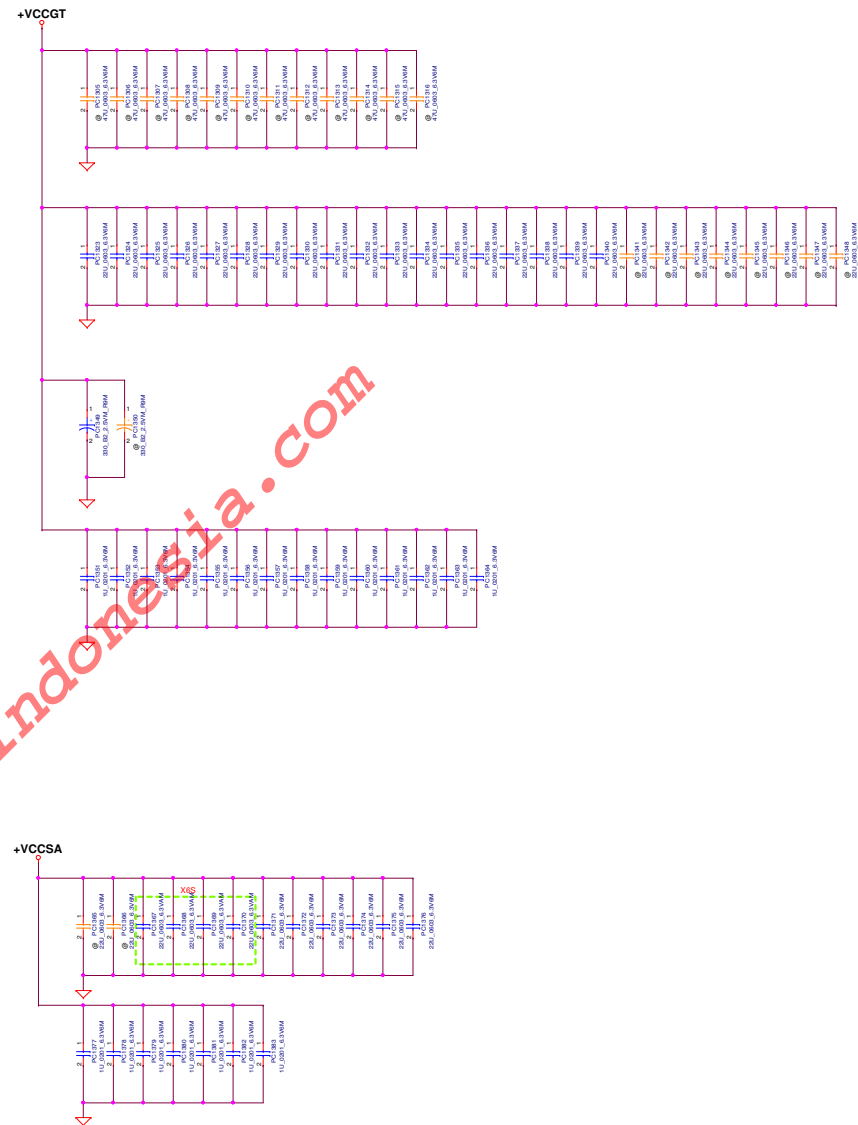
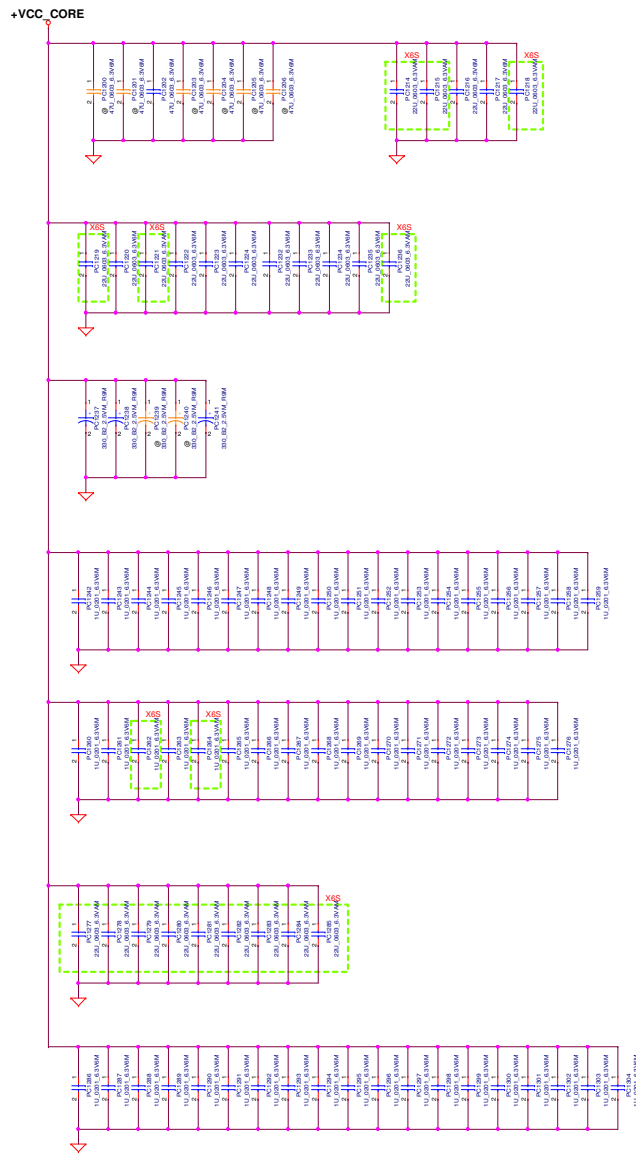
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VCC\_GT/SA Dr. MOS (36.2), Support component(36.3)



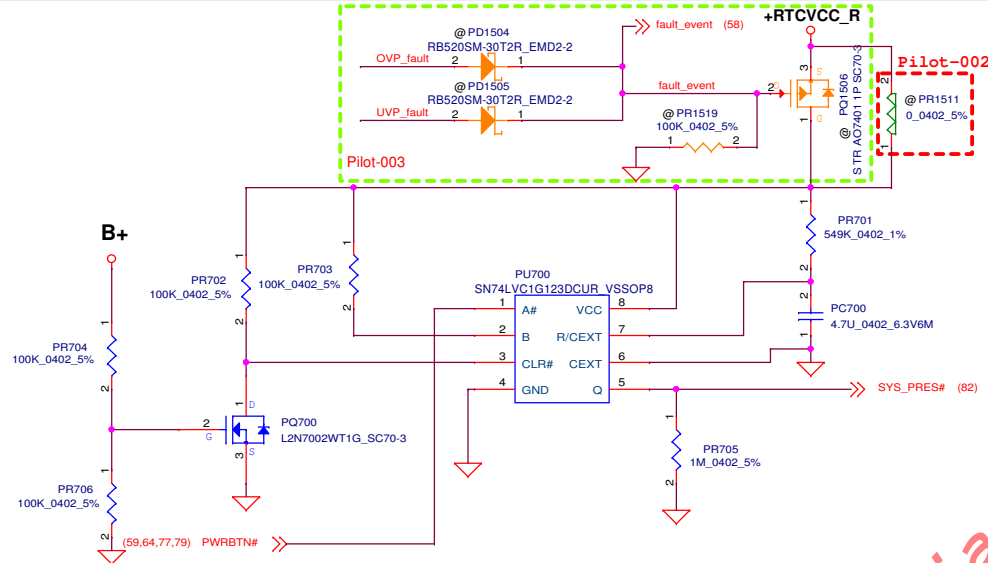
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VCC\_Core Output Cap(36.4), VCCGT Output Cap(36.5), VCCSA Output Cap(36.6)



VCC\_CORE output cap(36.4), VCC\_GT output cap(36.5), VCC\_SA output cap(36.6)

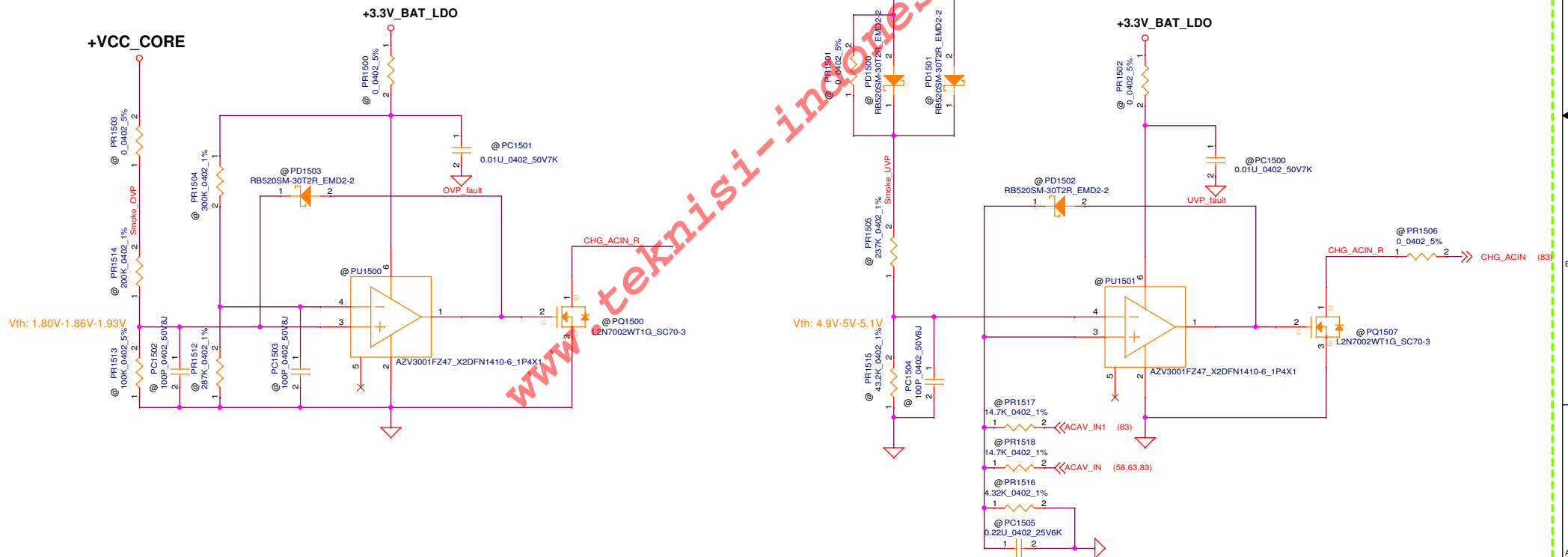
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1		2		3	



FUNCTION TABLE

INPUTS			OUTPUTS Q
CLR	$\bar{A}$	B	
L	X	X	L
X	H	X	L <sup>(1)</sup>
X	X	L	L <sup>(1)</sup>
H	L	↑	□
H	↓	H	□
↑	L	H	□

Pilot-003



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